Apéndice

Hojas de características de componentes

I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

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BC546/548

SILICON PLANAR EPITAXIAL TRANSISTORS

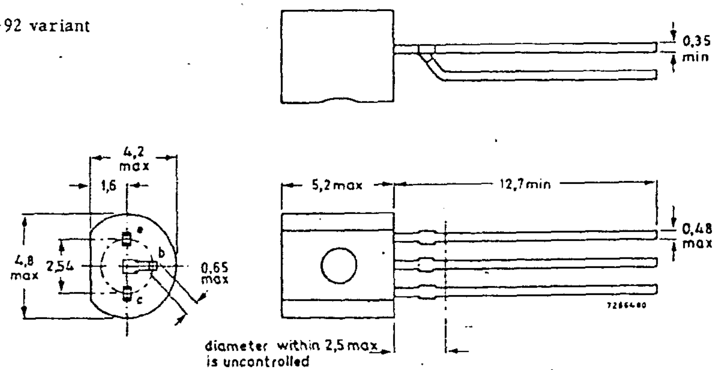
General purpose n-p-n transistors in a plastic TO-92 variant, especially suitable for use in driver stages of audio amplifiers.

QUICK REFERENCE DATA						
			BC546	BC547	BC548	
Collector-emitter voltage (V_{BE} = 0)	V_{CES}	max.	80	50	30	V
Collector-emitter voltage (open base)	V_{CEO}	max.	65	45	30	V
Collector current (peak value)	I_{CM}	max.	200	200	200	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	500	500	500	mW
Junction temperature	T_j	max.	150	150	150	°C
Small-signal current gain I_C = 2 mA; V_{CE} = 5 V; f = 1 kHz	h_{fe}	> <	125 500	125 900	125 900	
Transition frequency I_C = 10 mA; V_{CE} = 5 V	f_T	typ.	300	300	300	MHz
Noise figure at R_S = 2 kΩ I_C = 200 µA; V_{CE} = 5 V f = 1 kHz; B = 200 Hz	F	typ.	2	2	2	dB

MECHANICAL DATA

Dimensions in mm

TO-92 variant



Accessories: 56356 (cooling clip).

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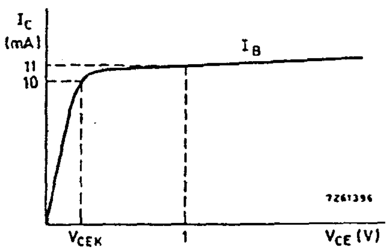
BC546/548

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current				
I_E = 0; V_{CB} = 30 V	I_{CBO}	<	15	nA
I_E = 0; V_{CB} = 30 V; T_j = 150 °C	I_{CBO}	<	5	μA
Base-emitter voltage 1)				
I_C = 2 mA; V_{CE} = 5 V	V_{BE}	typ.	660	mV
			580 to 700	mV
I_C = 10 mA; V_{CE} = 5 V	V_{BE}	<	770	mV
Saturation voltage 2)				
I_C = 10 mA; I_B = 0.5 mA	V_{CEsat}	typ.	90	mV
		<	250	mV
	V_{BEsat}	typ.	700	mV
I_C = 100 mA; I_B = 5 mA	V_{CEsat}	typ.	200	mV
		<	600	mV
	V_{BEsat}	typ.	900	mV
Knee voltage				
I_C = 10 mA; I_B = value for which I_C = 11 mA at V_{CE} = 1 V	V_{CEK}	typ.	300	mV
		<	600	mV



Collector capacitance at f = 1 MHz				
I_E = I_e = 0; V_{CB} = 10 V	C_c	typ.	2.5	pF
		<	4.5	pF
Emitter capacitance at f = 1 MHz				
I_C = I_c = 0; V_{EB} = 0.5 V	C_e	typ.	9	pF
Transition frequency at f = 35 MHz				
I_C = 10 mA; V_{CE} = 5 V	f_T	typ.	300	MHz

1) V_{BE} decreases by about 2 mV/°C with increasing temperature.
2) V_{BEsat} decreases by about 1,7 mV/°C with increasing temperature.

CHARACTERISTICS (continued)

T_j = 25 °C unless otherwise specified

			BC546	BC547	BC548	
Small signal current gain at f = 1 kHz						
I_C = 2 mA; V_{CE} = 5 V	h_{fe}	>	125	125	125	
		<	500	900	900	
Noise figure at R_S = 2 kΩ						
I_C = 200 μA; V_{CE} = 5 V	F	typ.	2	2	2	dB
f = 1 kHz; B = 200 Hz		<	10	10	10	dB

			BC546A BC547A BC548A	BC546B BC547B BC548B	BC547C BC548C	
D.C. current gain						
I_C = 10 μA; V_{CE} = 5 V	h_{FE}	typ.	90	150	270	
I_C = 2 mA; V_{CE} = 5 V	h_{FE}	>	110	200	420	
		typ.	180	290	520	
		<	220	450	800	
h parameters at f = 1 kHz (common emitter)						
I_C = 2 mA; V_{CE} = 5 V						
Input impedance	h_{ie}	>	1,6	3,2	6	kΩ
		typ.	2,7	4,5	8,7	kΩ
		<	4,5	8,5	15	kΩ
Reverse voltage transfer ratio	h_{re}	typ.	1,5	2	3	10^{-4}
Small signal current gain	h_{fe}	>	125	240	450	
		typ.	220	330	600	
		<	260	500	900	
Output admittance	h_{oe}	typ.	18	30	60	μA/V
		<	30	60	110	μA/V

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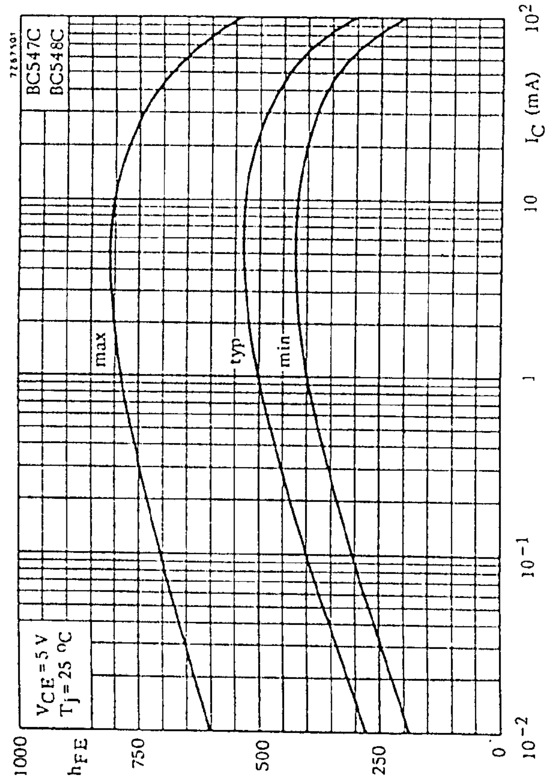

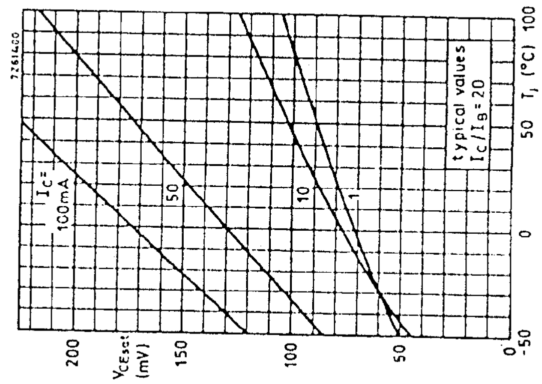

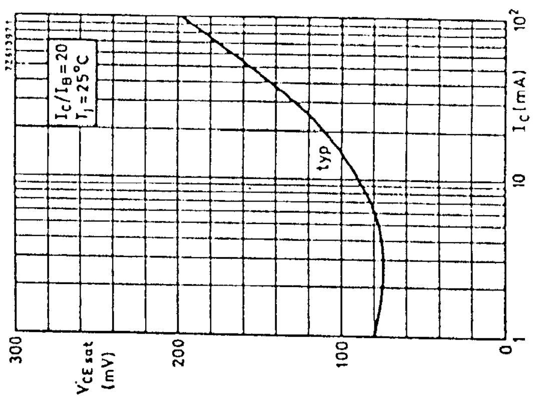

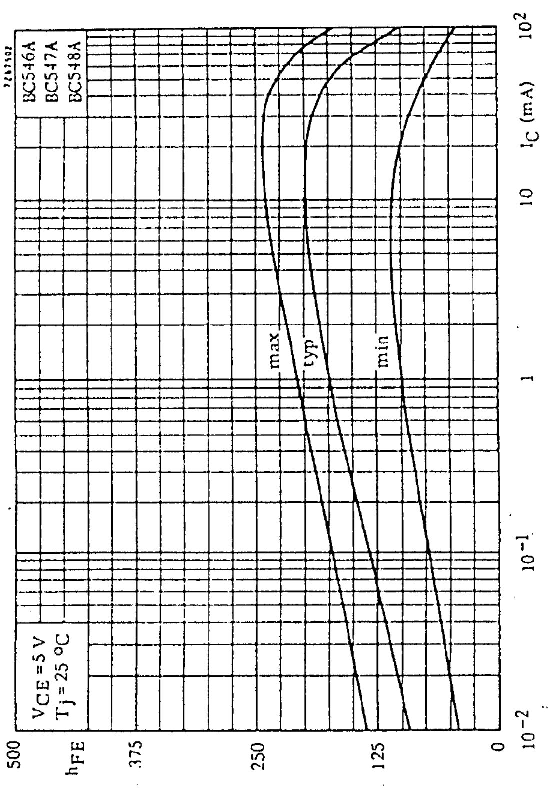

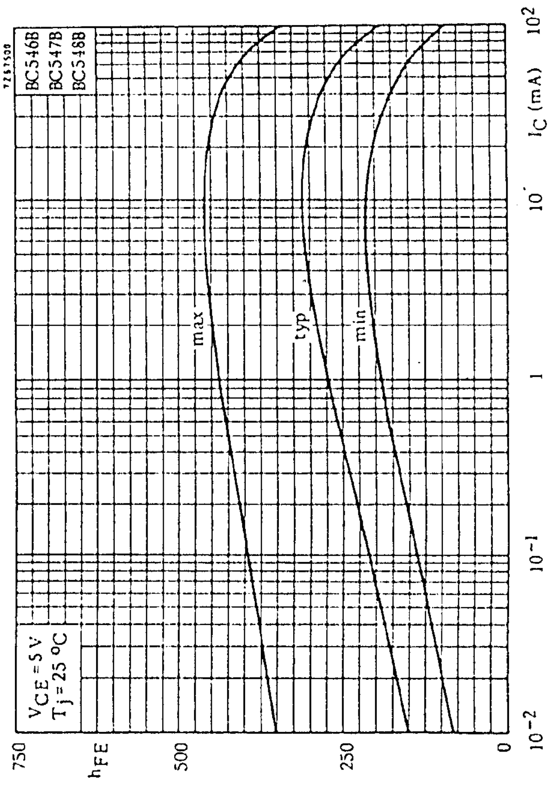

BC546/548

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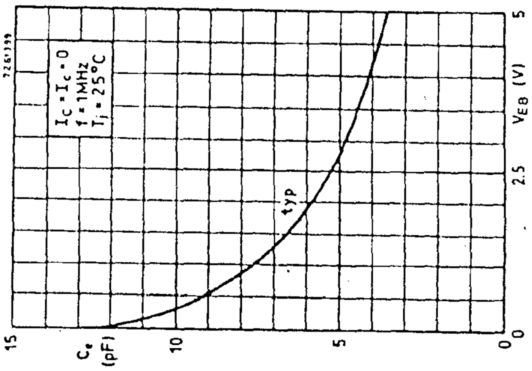

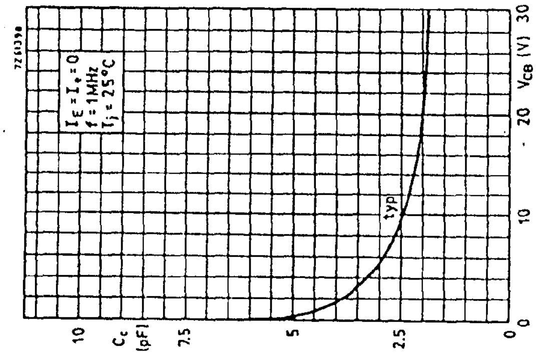

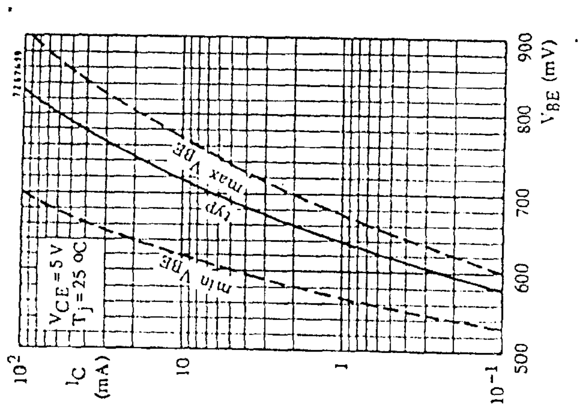

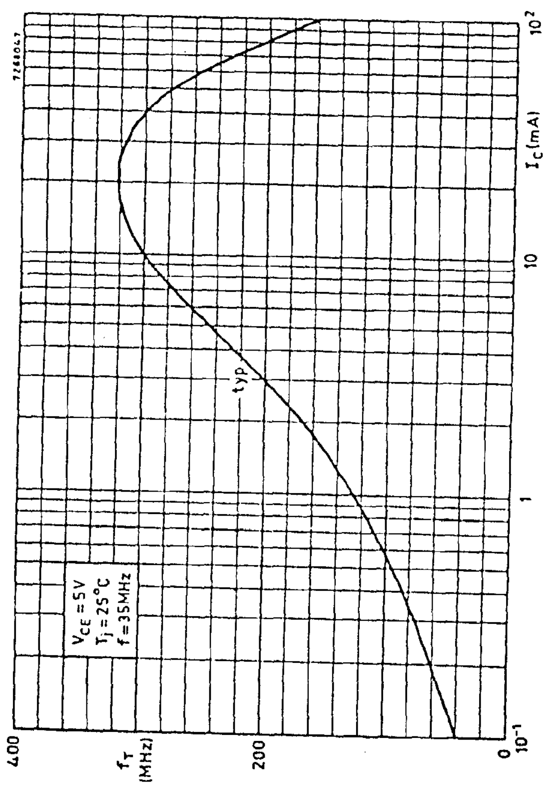

BC546/548

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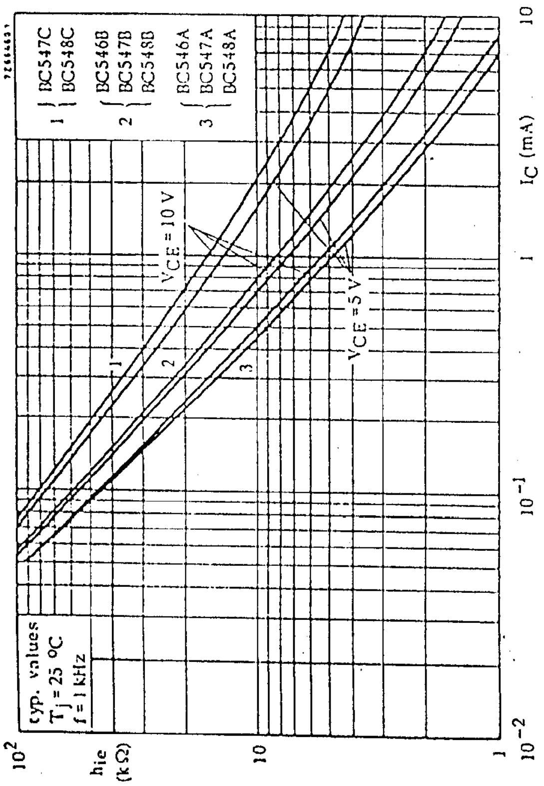
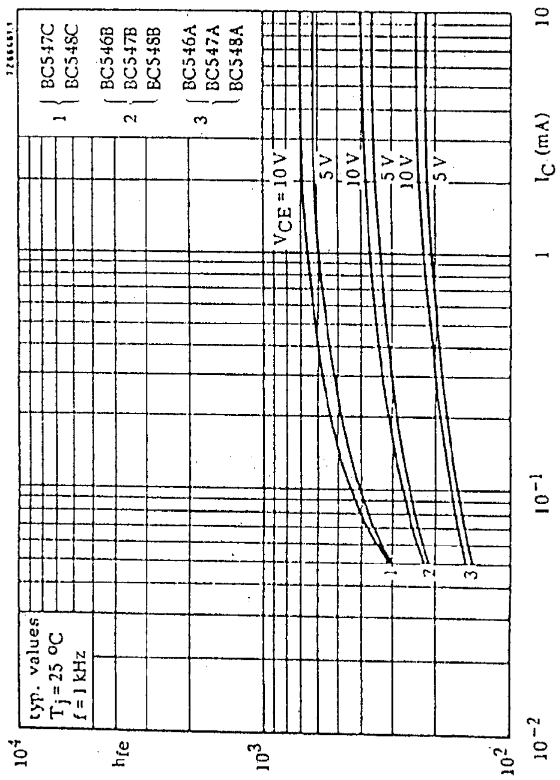
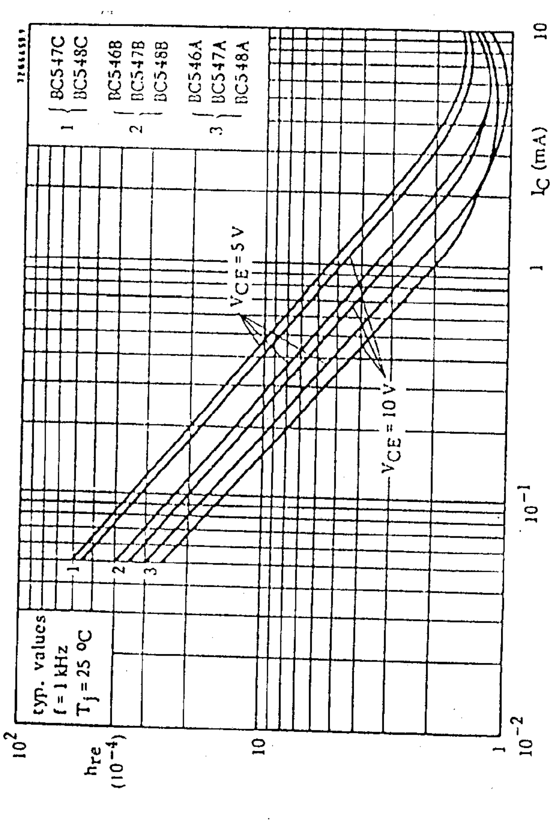
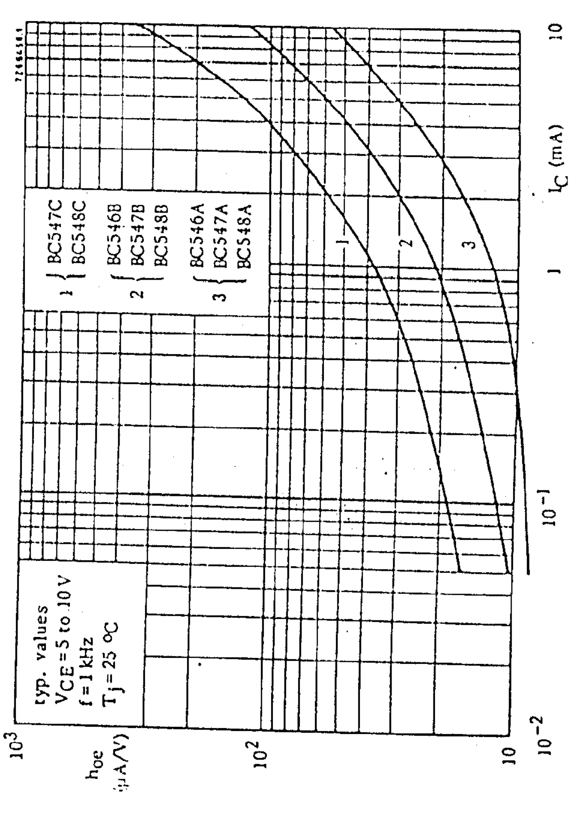

typ. values
T_j = 25 °C
f = 1 kHz
h_{ie} (kΩ)
1 { BC547C BC548C
2 { BC546B BC547B BC548B
3 { BC546A BC547A BC548A
V_{CE} = 10 V
V_{CE} = 5 V
I_C (mA)


typ. values
T_j = 25 °C
f = 1 kHz
h_{fe}
1 { BC547C BC548C
2 { BC546B BC547B BC548B
3 { BC546A BC547A BC548A
V_{CE} = 10 V
5 V
10 V
5 V
10 V
5 V
I_C (mA)


typ. values
f = 1 kHz
T_j = 25 °C
h_{re} (10^{-4})
1 { BC547C BC548C
2 { BC546B BC547B BC548B
3 { BC546A BC547A BC548A
V_{CE} = 5 V
V_{CE} = 10 V
I_C (mA)


typ. values
V_{CE} = 5 to 10 V
f = 1 kHz
T_j = 25 °C
h_{oe} (μA/V)
1 { BC547C BC548C
2 { BC546B BC547B BC548B
3 { BC546A BC547A BC548A
I_C (mA)

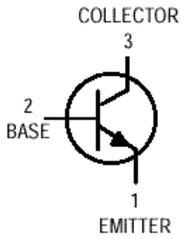
BC546/548

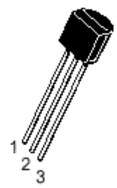
General Purpose Transistors

NPN Silicon

2N3903
2N3904*

*Motorola Preferred Device





CASE 29–04, STYLE 1
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS(1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (2) (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	—	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	60	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	6.0	—	Vdc
Base Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	I_{BL}	—	50	nAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	I_{CEX}	—	50	nAdc

1. Indicates Data in addition to JEDEC Requirements.
2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain(1)		h_{FE}			—
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	2N3903		20	—	
	2N3904		40	—	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3903		35	—	
	2N3904		70	—	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3903		50	150	
	2N3904		100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3903		30	—	
	2N3904		60	—	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3903		15	—	
	2N3904		30	—	
Collector–Emitter Saturation Voltage(1)		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			—	0.2	
(I_C = 50 mAdc, I_B = 5.0 mAdc			—	0.3	
Base–Emitter Saturation Voltage(1)		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			0.65	0.85	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			—	0.95	
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N3903		250	—	
	2N3904		300	—	
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	—	4.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	—	8.0	pF
Input Impedance		h_{ie}			k Ω
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		1.0	8.0	
	2N3904		1.0	10	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		0.1	5.0	
	2N3904		0.5	8.0	
Small–Signal Current Gain		h_{fe}			—
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903		50	200	
	2N3904		100	400	
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{oe}	1.0	40	μmhos
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	2N3903		—	6.0	
	2N3904		—	5.0	

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = 0.5 Vdc, I_C = 10 mAdc, I_{B1} = 1.0 mAdc)		t_d	—	35	ns
Rise Time			t_r	—	35	ns
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 1.0 mAdc)	2N3903	t_s	—	175	ns
		2N3904		—	200	
Fall Time			t_f	—	50	ns

1. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

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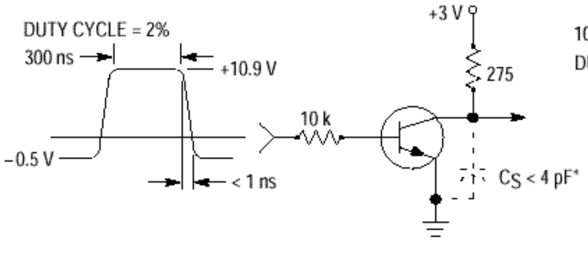

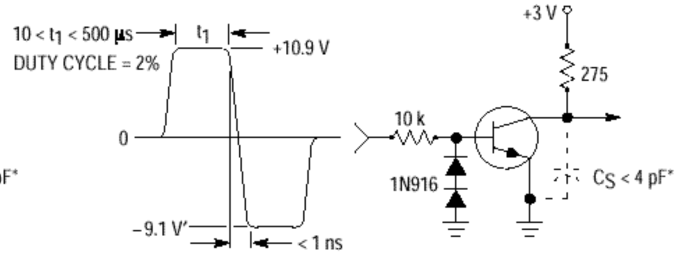

* Total shunt capacitance of test jig and connectors

Figure 1. Delay and Rise Time Equivalent Test Circuit

Figure 2. Storage and Fall Time Equivalent Test Circuit

TYPICAL TRANSIENT CHARACTERISTICS

T_J = 25°C
T_J = 125°C

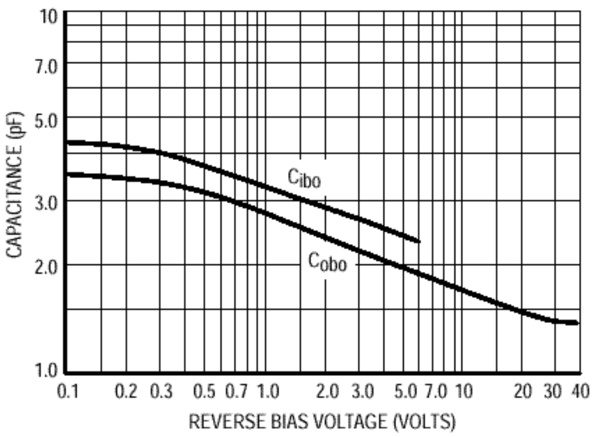

Figure 3. Capacitance

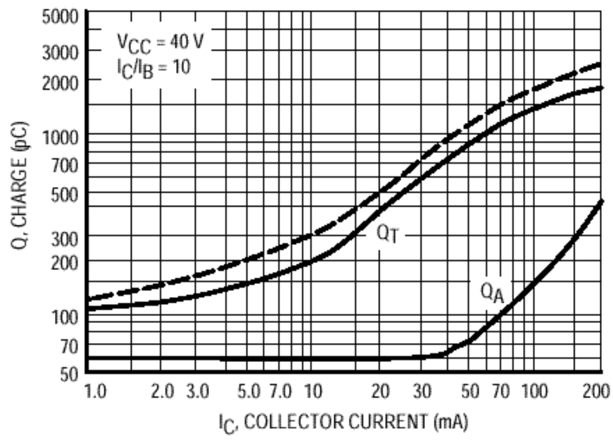

Figure 4. Charge Data

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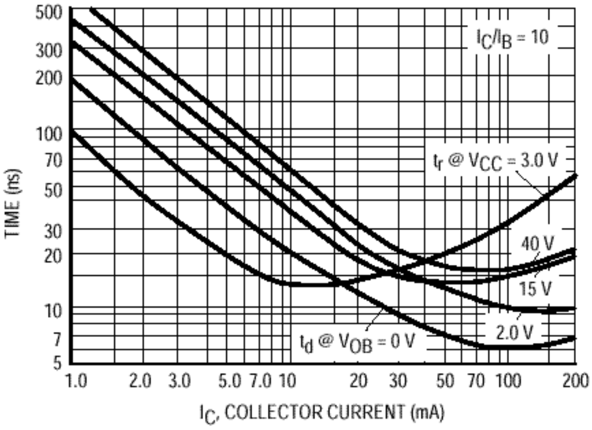

Figure 5. Turn−On Time

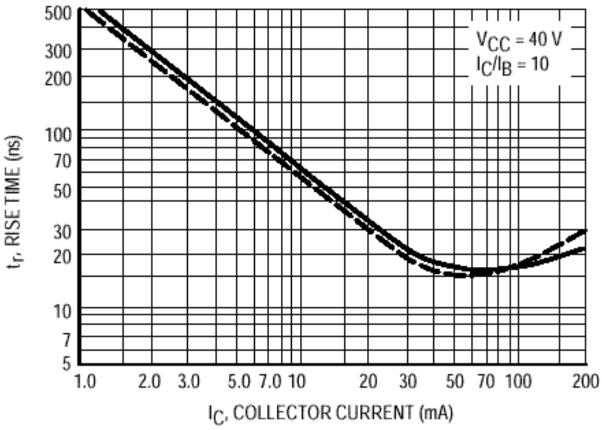

Figure 6. Rise Time

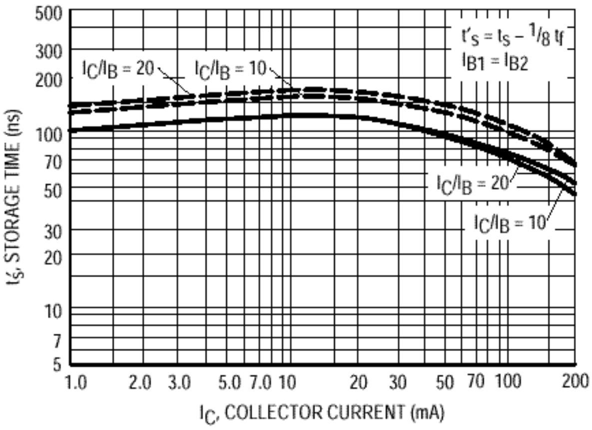

Figure 7. Storage Time

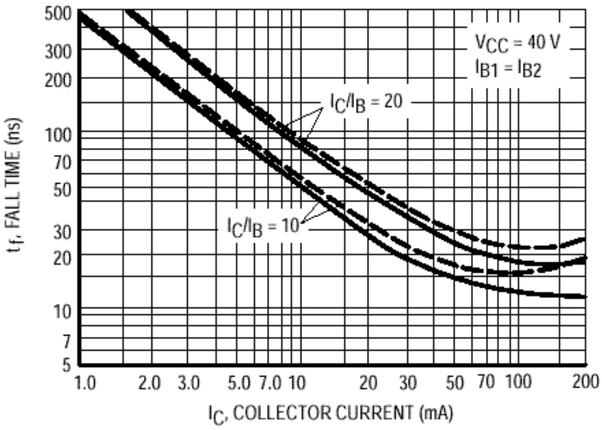

Figure 8. Fall Time

TYPICAL AUDIO SMALL−SIGNAL CHARACTERISTICS
NOISE FIGURE VARIATIONS

(V_{CE} = 5.0 Vdc, T_A = 25°C, Bandwidth = 1.0 Hz)

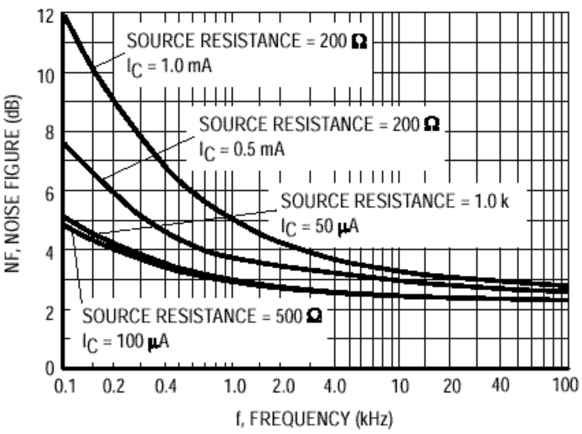

Figure 9.

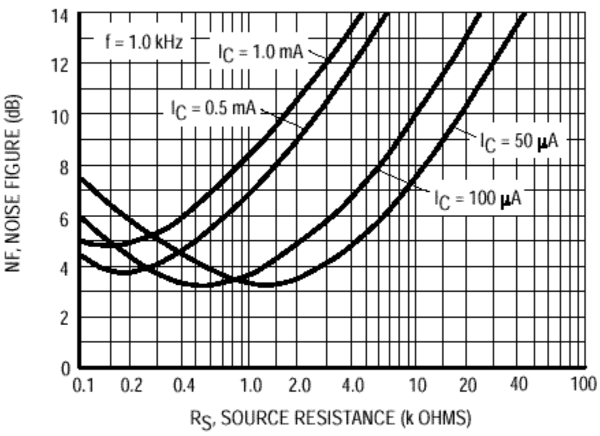

Figure 10.

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h PARAMETERS
(V_{CE} = 10 Vdc, f = 1.0 kHz, T_A = 25°C)

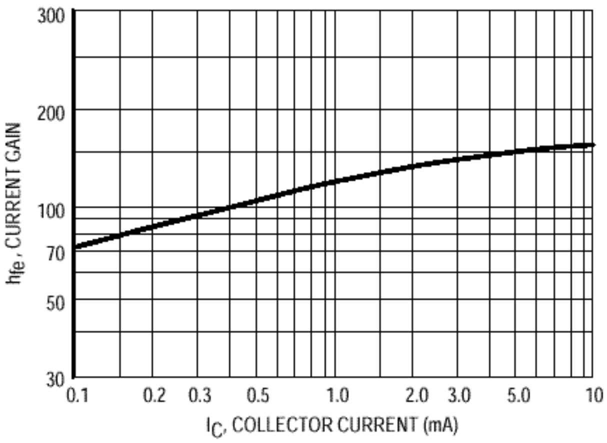

Figure 11. Current Gain

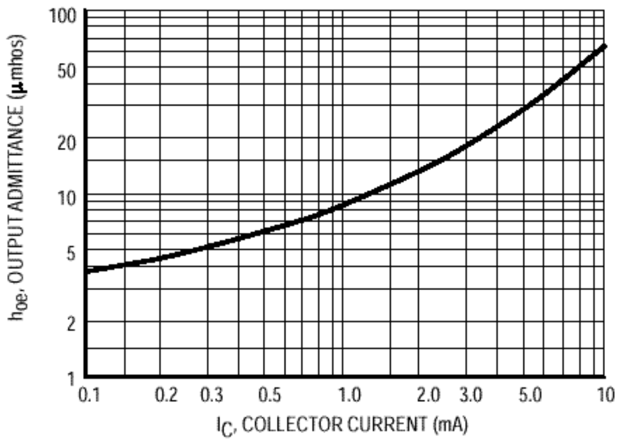

Figure 12. Output Admittance

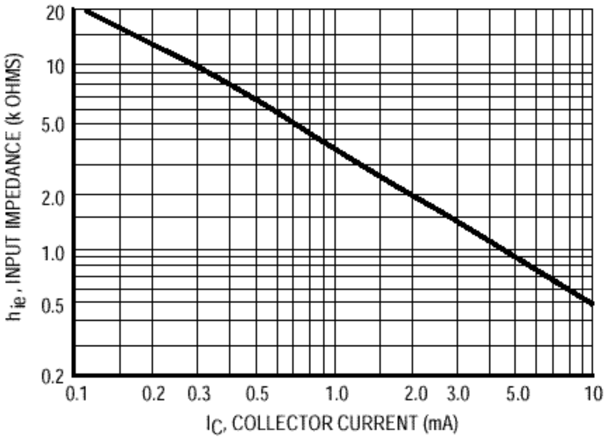

Figure 13. Input Impedance

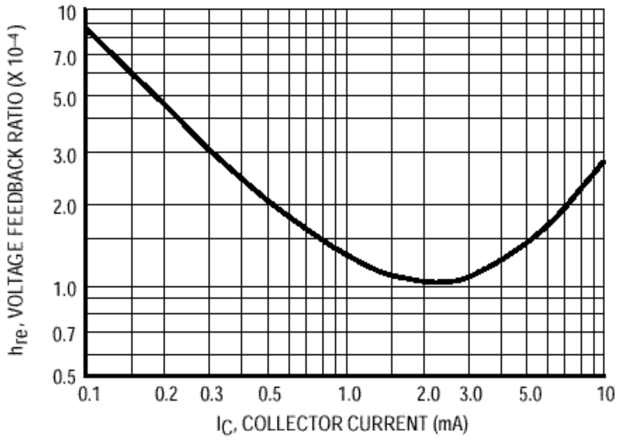

Figure 14. Voltage Feedback Ratio

TYPICAL STATIC CHARACTERISTICS

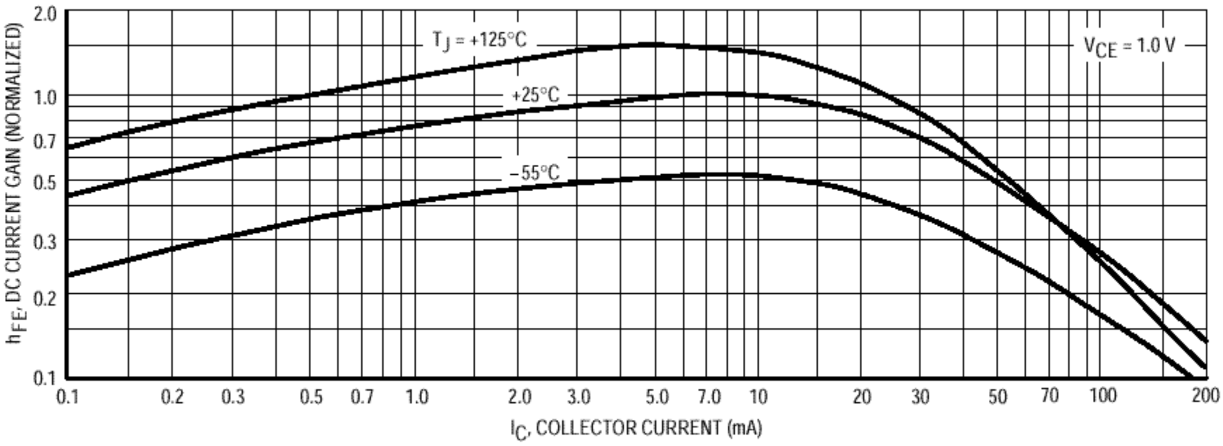

Figure 15. DC Current Gain

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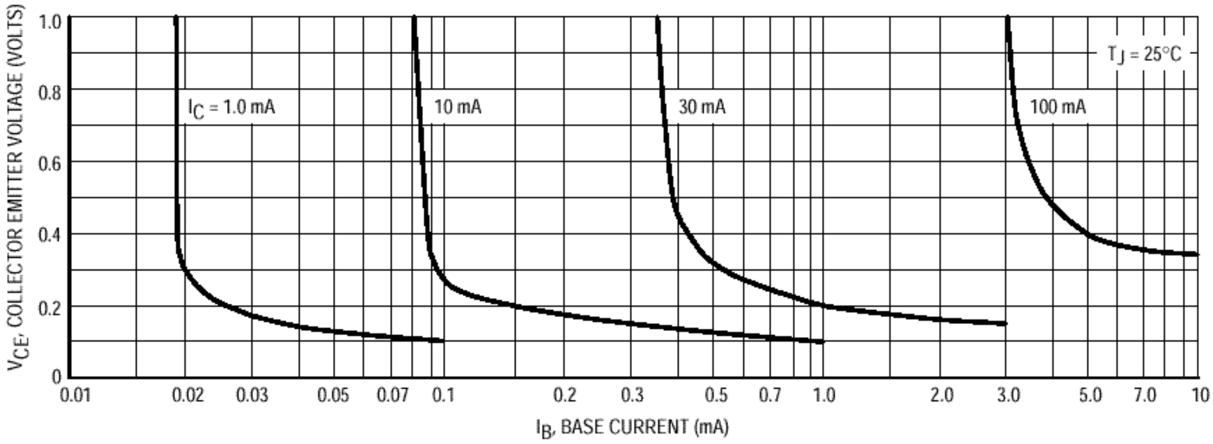

Figure 16. Collector Saturation Region

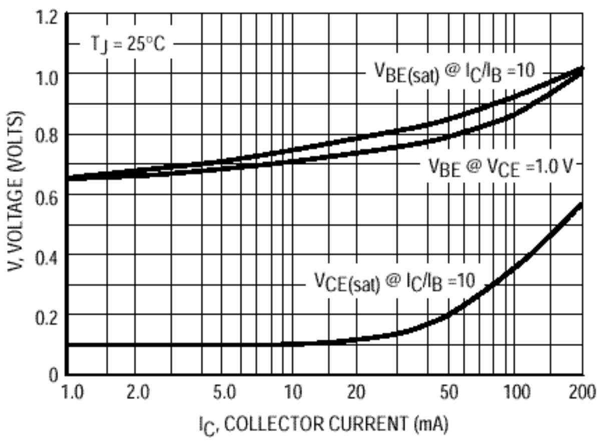

Figure 17. "ON" Voltages

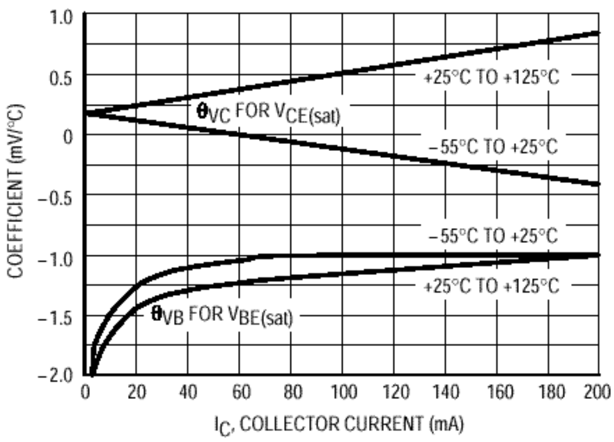

Figure 18. Temperature Coefficients

2N3903/04

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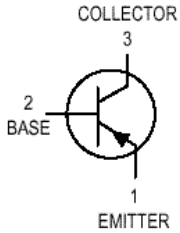
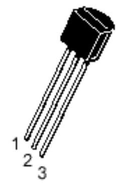
General Purpose Transistors

PNP Silicon

2N3905
2N3906*

*Motorola Preferred Device





CASE 29–04, STYLE 1
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CBO}	40	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Power Dissipation @ T_A = 60°C	P_D	250	mW
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS(1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (2) (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	—	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	40	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	—	Vdc
Base Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	I_{BL}	—	50	nAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	I_{CEX}	—	50	nAdc

1. Indicates Data in addition to JEDEC Requirements.
2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS[1]					
DC Current Gain		h_{FE}			—
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	2N3905		30	—	
	2N3906		60	—	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3905		40	—	
	2N3906		80	—	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3905		50	150	
	2N3906		100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3905		30	—	
	2N3906		60	—	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3905		15	—	
	2N3906		30	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			—	0.25	
(I_C = 50 mAdc, I_B = 5.0 mAdc			—	0.4	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			0.65	0.85	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			—	0.95	
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N3905		200	—	
	2N3906		250	—	
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	—	4.5	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	—	10.0	pF
Input Impedance		h_{ie}			k Ω
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3905		0.5	8.0	
	2N3906		2.0	12	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3905		0.1	5.0	
	2N3906		0.1	10	
Small–Signal Current Gain		h_{fe}			—
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3905		50	200	
	2N3906		100	400	
Output Admittance		h_{oe}			μmhos
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3905		1.0	40	
	2N3906		3.0	60	
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	2N3905		—	5.0	
	2N3906		—	4.0	

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = 0.5 Vdc, I_C = 10 mAdc, I_{B1} = 1.0 mAdc)		t_d	—	35	ns
Rise Time			t_r	—	35	ns
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 1.0 mAd	2N3905	t_s	—	200	ns
		2N3906		—	225	
Fall Time		2N3905	t_f	—	60	ns
		2N3906		—	75	

1. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

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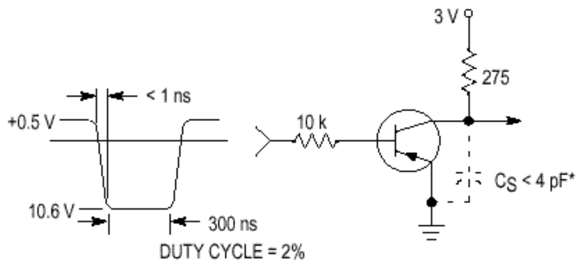
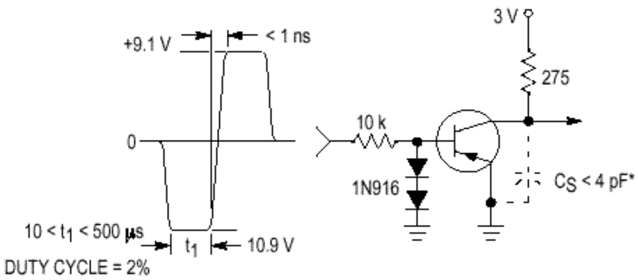


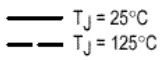


* Total shunt capacitance of test jig and connectors

Figure 1. Delay and Rise Time Equivalent Test Circuit

Figure 2. Storage and Fall Time Equivalent Test Circuit

TYPICAL TRANSIENT CHARACTERISTICS



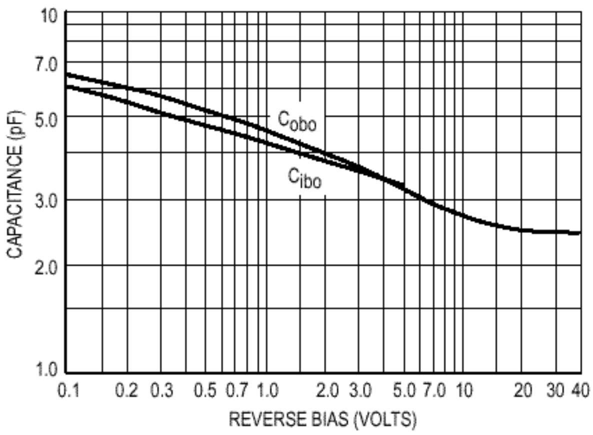


Figure 3. Capacitance

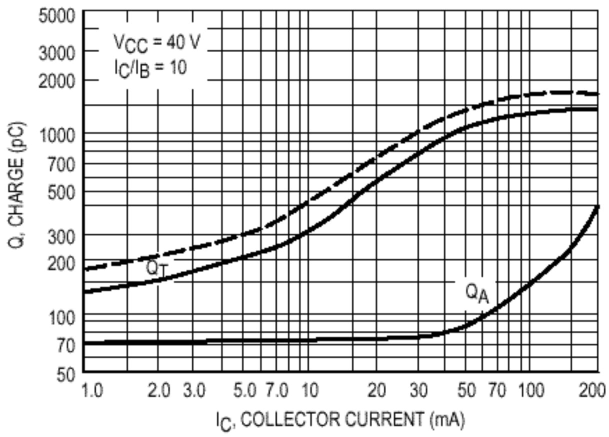


Figure 4. Charge Data

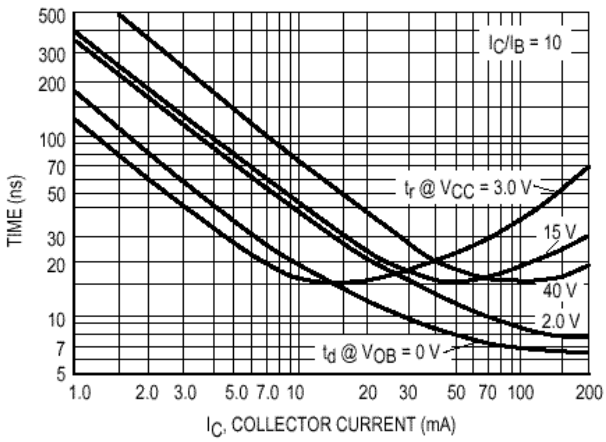


Figure 5. Turn−On Time

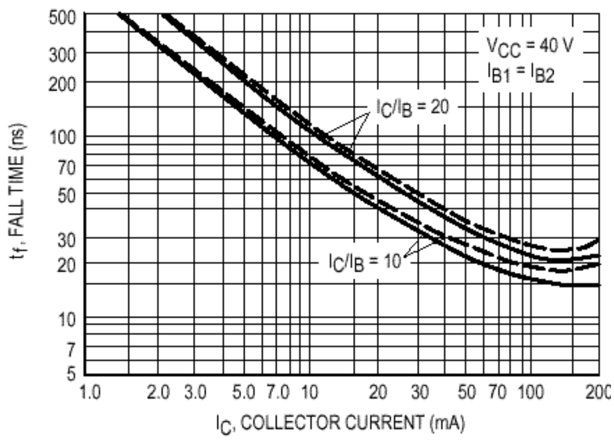


Figure 6. Fall Time

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TYPICAL AUDIO SMALL–SIGNAL CHARACTERISTICS
NOISE FIGURE VARIATIONS

(V_{CE} = –5.0 Vdc, T_A = 25°C, Bandwidth = 1.0 Hz)

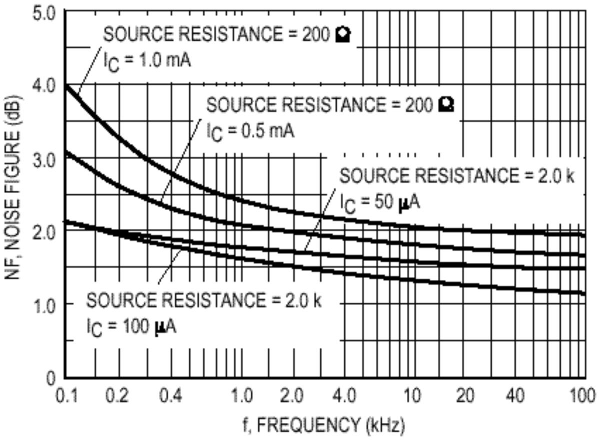

Figure 7.

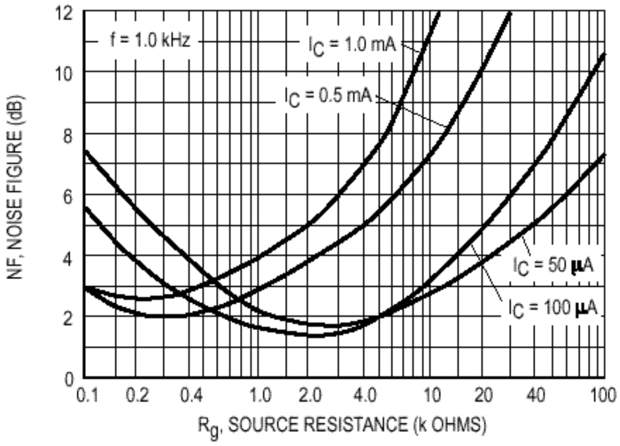

Figure 8.

h PARAMETERS

(V_{CE} = –10 Vdc, f = 1.0 kHz, T_A = 25°C)

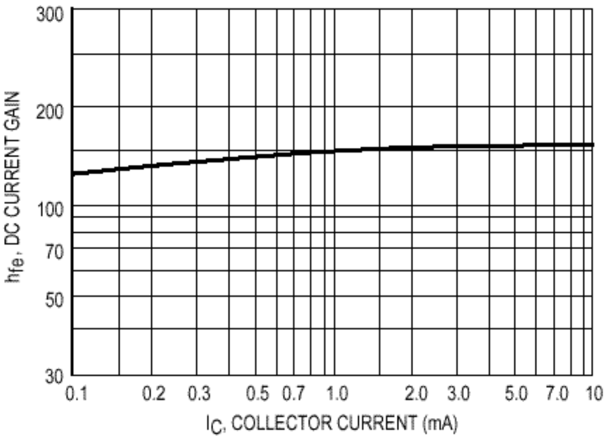

Figure 9. Current Gain

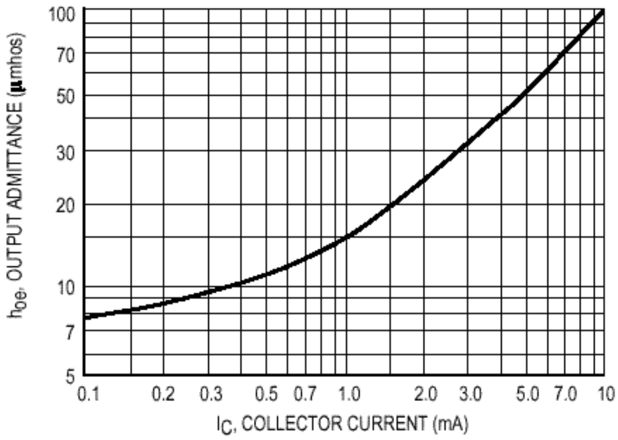

Figure 10. Output Admittance

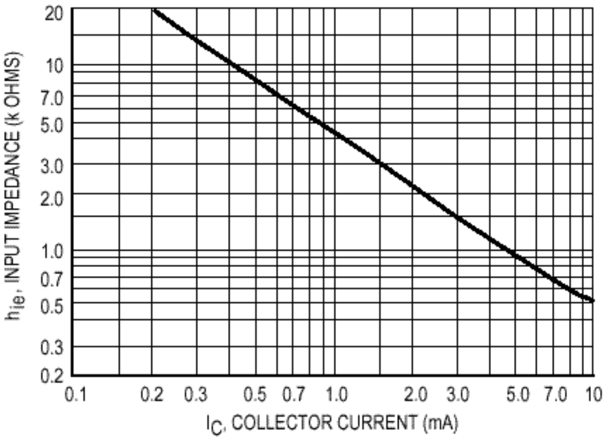

Figure 11. Input Impedance

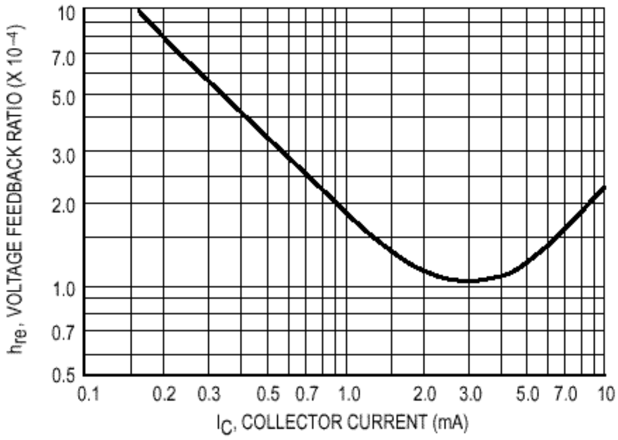

Figure 12. Voltage Feedback Ratio

2N3905/06

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TYPICAL STATIC CHARACTERISTICS

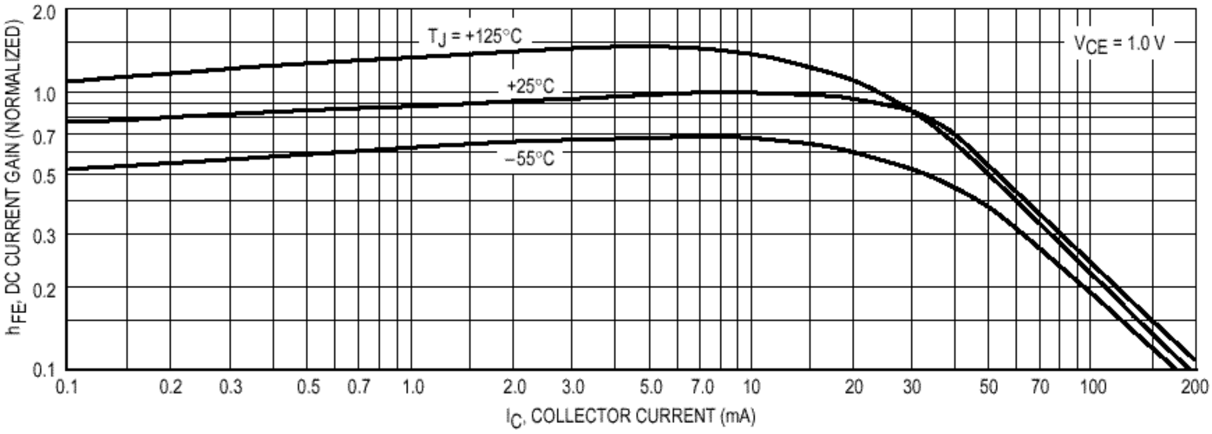

Figure 13. DC Current Gain

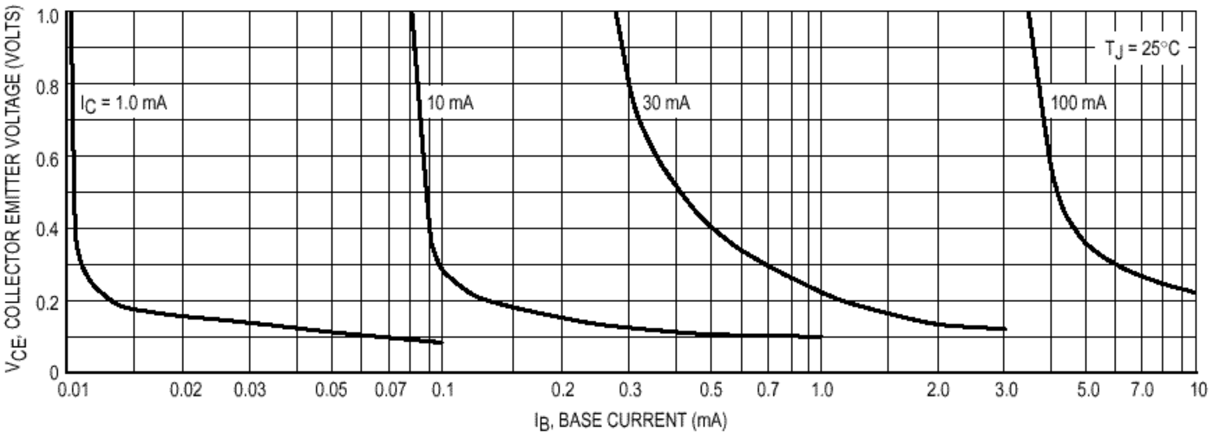

Figure 14. Collector Saturation Region

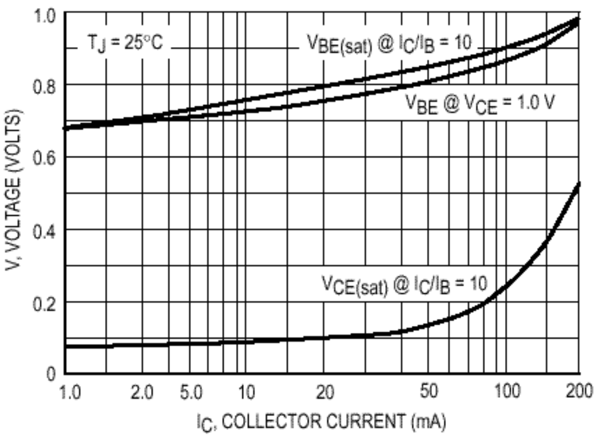

Figure 15. "ON" Voltages

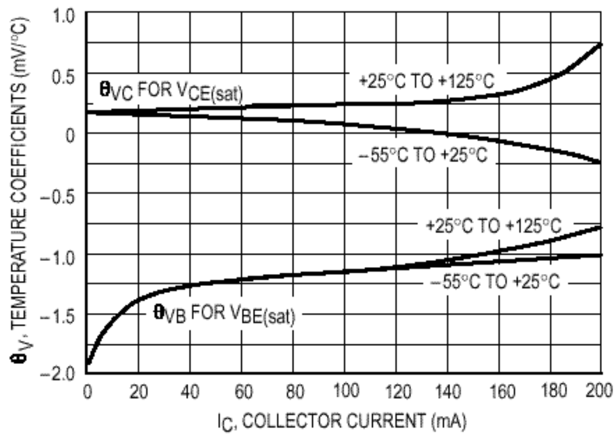

Figure 16. Temperature Coefficients

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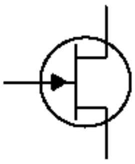
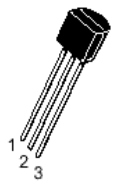
JFETs — General Purpose

N–Channel — Depletion



2N5457

*Motorola Preferred Device



CASE 29–04, STYLE 5
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	25	Vdc
Reverse Gate–Source Voltage	V_{GSR}	–25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction Temperature Range	T_J	125	°C
Storage Channel Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Gate–Source Breakdown Voltage (I_G = –10 µAdc, V_{DS} = 0)	$V_{(BR)GSS}$	–25	—	—	Vdc
Gate Reverse Current (V_{GS} = –15 Vdc, V_{DS} = 0) (V_{GS} = –15 Vdc, V_{DS} = 0, T_A = 100°C)	I_{GSS}	 — —	 — —	 –1.0 –200	nAdc
Gate–Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	$V_{GS(off)}$	–0.5	—	–6.0	Vdc
Gate–Source Voltage (V_{DS} = 15 Vdc, I_D = 100 µAdc)	V_{GS}	—	–2.5	—	Vdc
ON CHARACTERISTICS					
Zero–Gate–Voltage Drain Current (1) (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	1.0	3.0	5.0	mAdc
SMALL–SIGNAL CHARACTERISTICS					
Forward Transfer Admittance Common Source (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|y_{fs}\|$	1000	—	5000	µmhos
Output Admittance Common Source (1) (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|y_{os}\|$	—	10	50	µmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	4.5	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	1.5	3.0	pF

1. Pulse Test; Pulse Width ≤ 630 ms, Duty Cycle ≤ 10%.

2N5457

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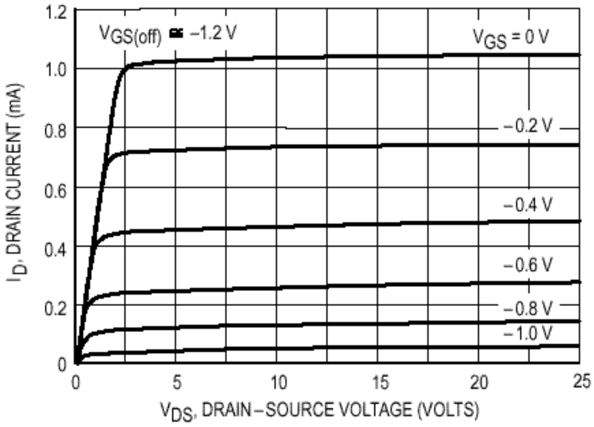

Figure 3. Typical Drain Characteristics

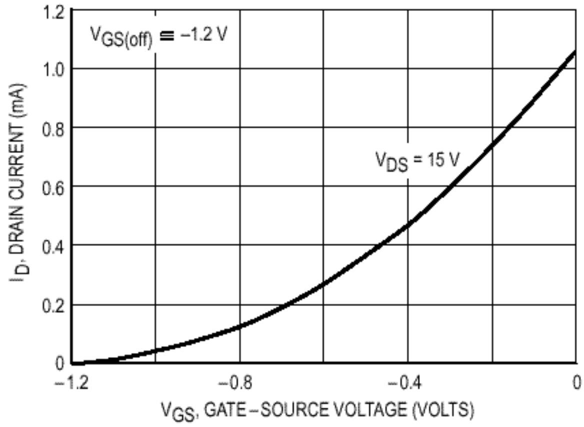

Figure 4. Common Source Transfer Characteristics

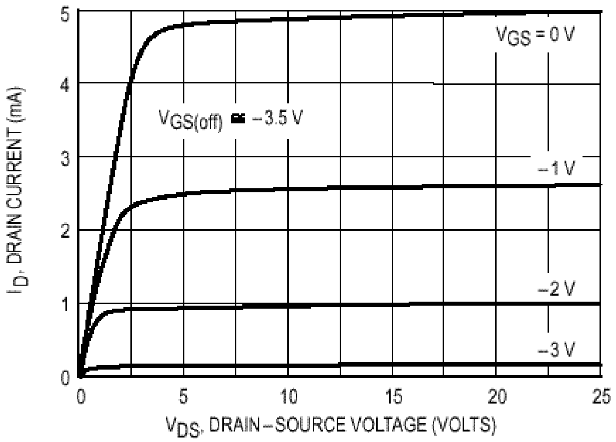

Figure 5. Typical Drain Characteristics

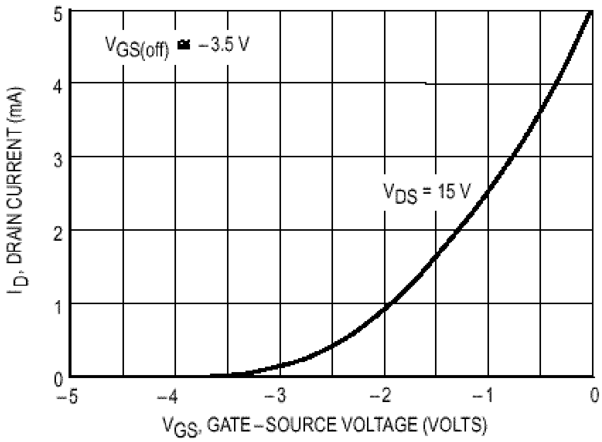

Figure 6. Common Source Transfer Characteristics

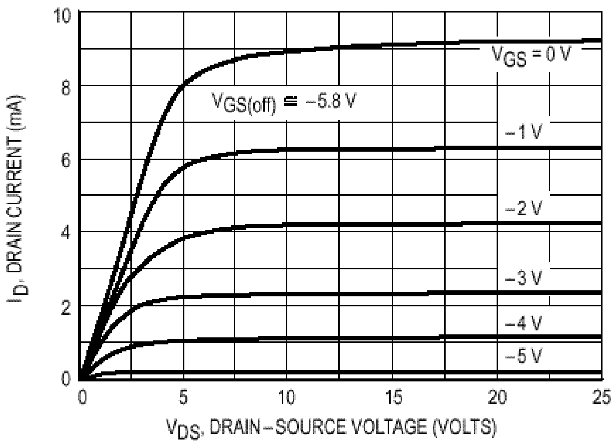

Figure 7. Typical Drain Characteristics

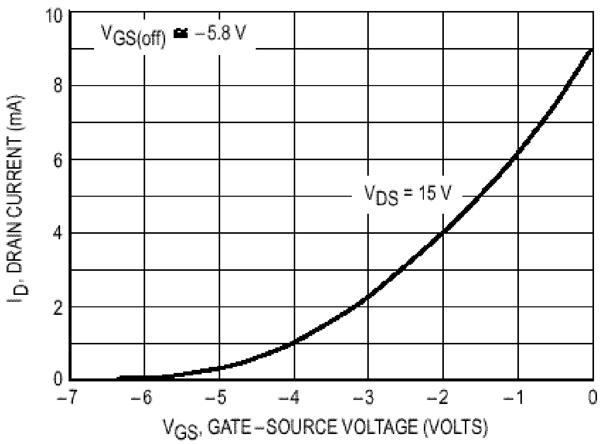

Figure 8. Common Source Transfer Characteristics

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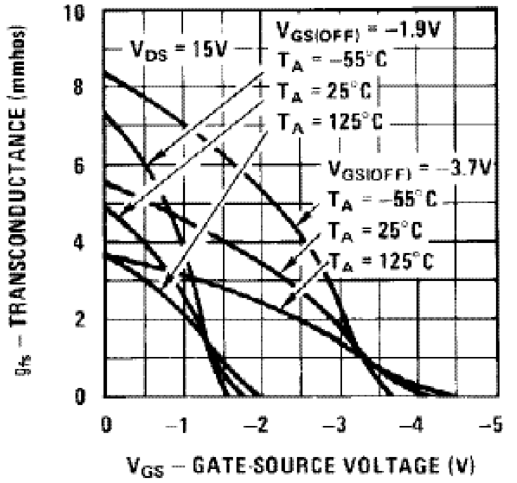
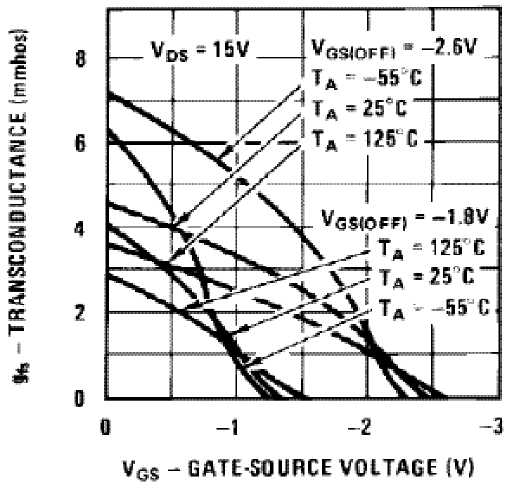
Typical Characteristics (continued)

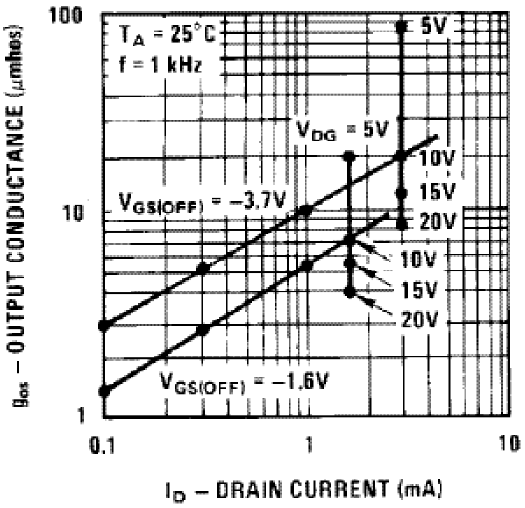
Transfer Characteristics



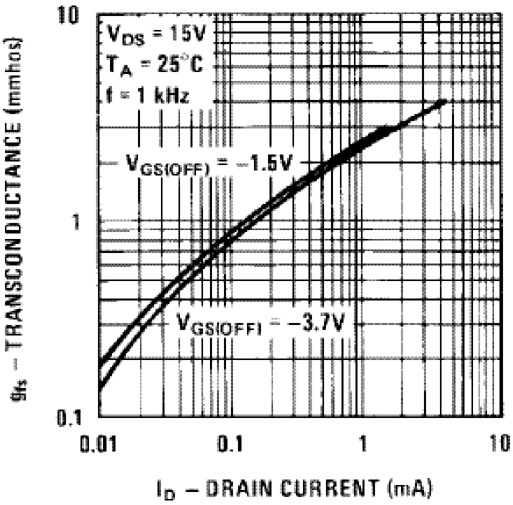
Transfer Characteristics



Output Conductance vs. Drain Current



Transconductance vs. Drain Current



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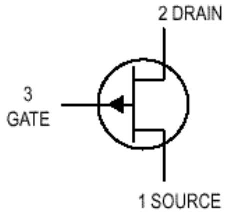
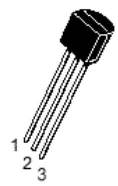
I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

JFET Amplifiers
P–Channel — Depletion



2N5460
thru
2N5462



CASE 29–04, STYLE 7
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Gate Voltage	V_{DG}	40	Vdc
Reverse Gate–Source Voltage	V_{GSR}	40	Vdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Junction Temperature Range	T_J	–65 to +135	°C
Storage Channel Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate–Source Breakdown Voltage (I_G = 10 µAdc, V_{DS} = 0)	 2N5460, 2N5461, 2N5462	$V_{(BR)GSS}$	40	—	—	Vdc
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0) (V_{GS} = 30 Vdc, V_{DS} = 0) (V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C) (V_{GS} = 30 Vdc, V_{DS} = 0, T_A = 100°C)	 2N5460, 2N5461, 2N5462 2N5460, 2N5461, 2N5462	I_{GSS}	 — —	 — —	 5.0 1.0	 nAdc µAdc
Gate–Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 µAdc)	2N5460 2N5461 2N5462	$V_{GS(off)}$	0.75 1.0 1.8	— — —	6.0 7.5 9.0	Vdc
Gate–Source Voltage (V_{DS} = 15 Vdc, I_D = 0.1 mAdc) (V_{DS} = 15 Vdc, I_D = 0.2 mAdc) (V_{DS} = 15 Vdc, I_D = 0.4 mAdc)	 2N5460 2N5461 2N5462	V_{GS}	 0.5 0.8 1.5	 — — —	 4.0 4.5 6.0	Vdc
ON CHARACTERISTICS						
Zero–Gate–Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5460 2N5461 2N5462	I_{DSS}	–1.0 –2.0 –4.0	— — —	–5.0 –9.0 –16	mAdc
SMALL–SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5460 2N5461 2N5462	$\|y_{fs}\|$	1000 1500 2000	— — —	4000 5000 6000	µmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\|y_{os}\|$	—	—	75	µmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	5.0	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	—	1.0	2.0	pF
FUNCTIONAL CHARACTERISTICS						
Noise Figure (V_{DS} = 15 Vdc, V_{GS} = 0, R_G = 1.0 Megohm, f = 100 Hz, BW = 1.0 Hz)		NF	—	1.0	2.5	dB
Equivalent Short–Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz)		e_n	—	60	115	$nV/\sqrt{Hz}$

2N5460/62

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DRAIN CURRENT versus GATE SOURCE VOLTAGE

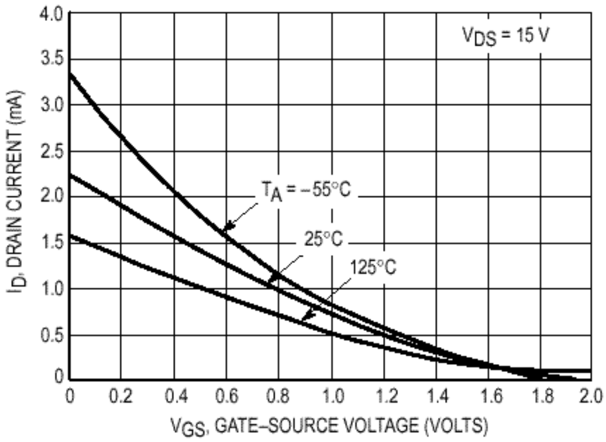

Figure 1. $V_{GS(off)}$ = 2.0 Volts

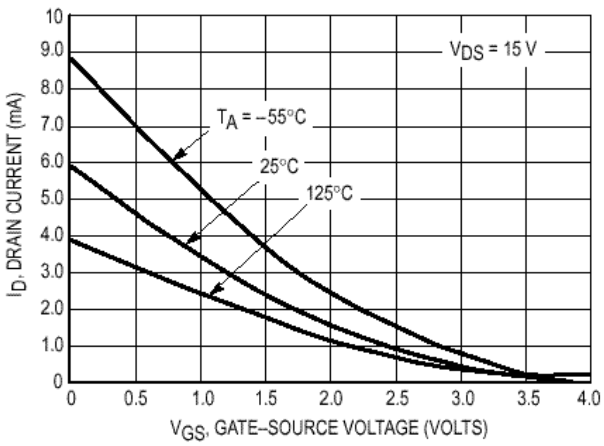

Figure 2. $V_{GS(off)}$ = 4.0 Volts

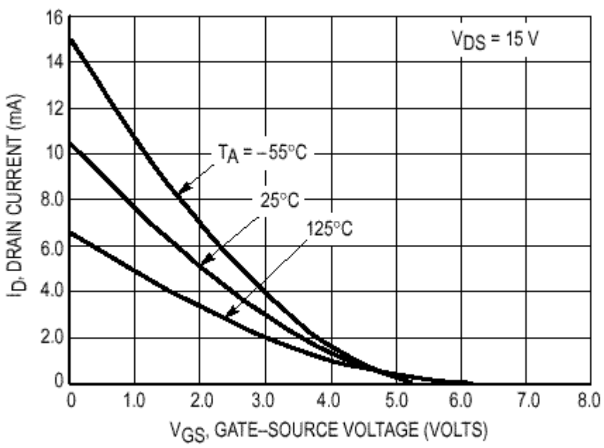

Figure 3. $V_{GS(off)}$ = 5.0 Volts

FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

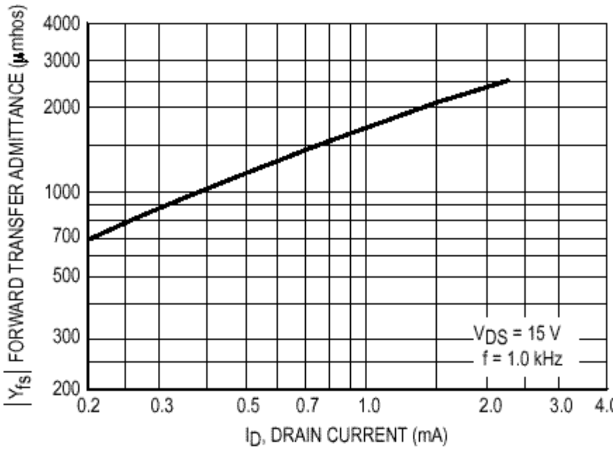

Figure 4. $V_{GS(off)}$ = 2.0 Volts

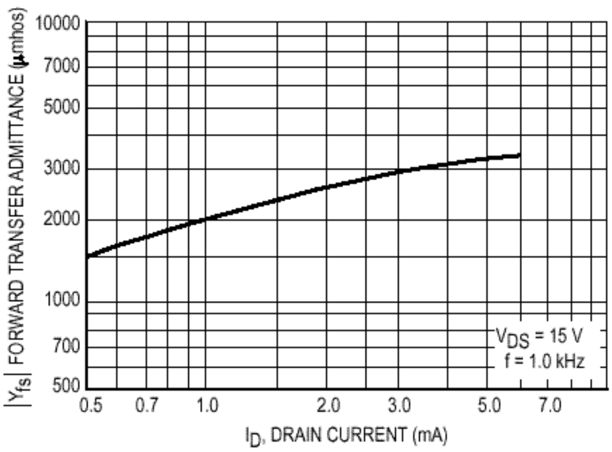

Figure 5. $V_{GS(off)}$ = 4.0 Volts

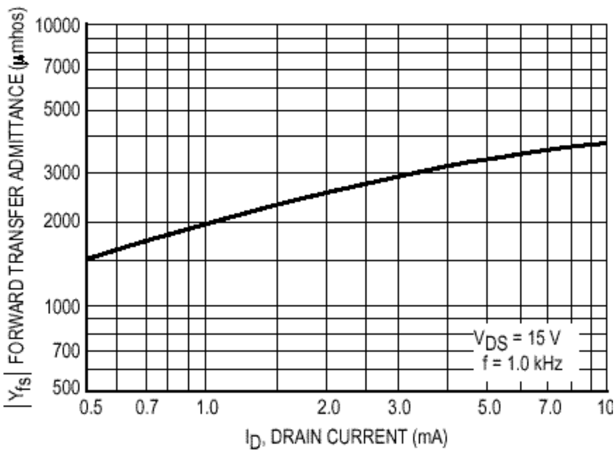

Figure 6. $V_{GS(off)}$ = 5.0 Volts

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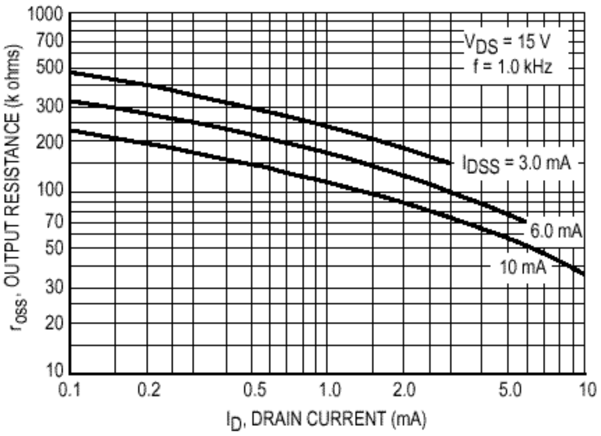


Figure 7. Output Resistance versus Drain Current

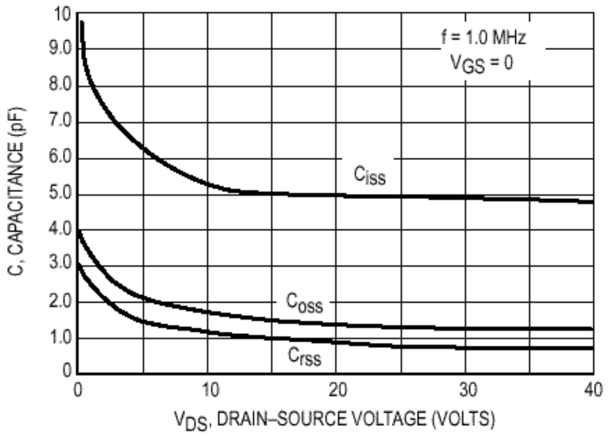


Figure 8. Capacitance versus Drain–Source Voltage

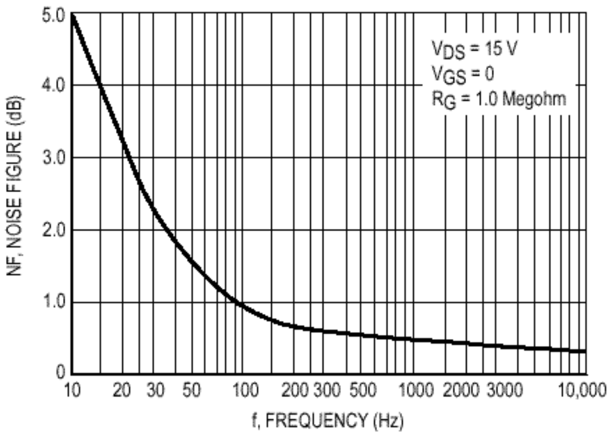


Figure 9. Noise Figure versus Frequency

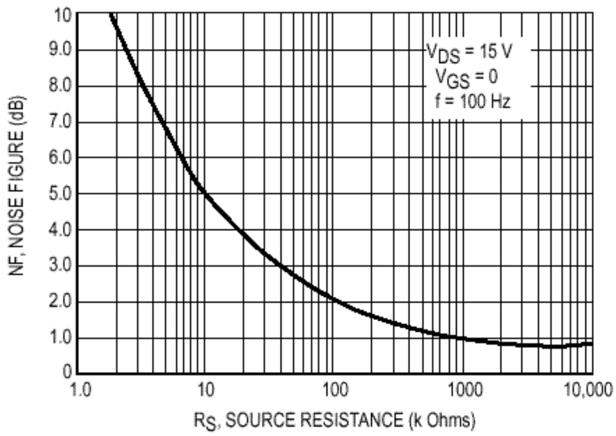
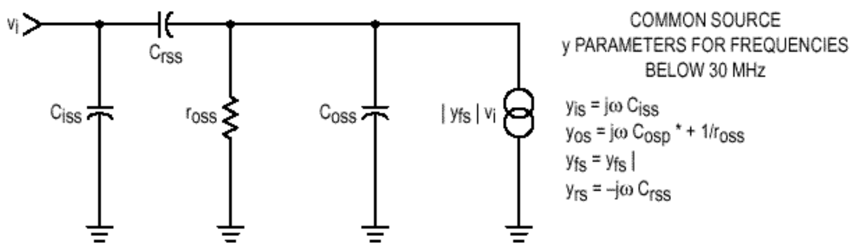


Figure 10. Noise Figure versus Source Resistance



* C_{osp} is C_{oss} in parallel with Series Combination of C_{iss} and C_{rss}.

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General purpose operational amplifier • A741/• A741C/SA741C

DESCRIPTION

The • A741 is a high performance operational amplifier with high open-loop gain, internal compensation, high common mode range and exceptional temperature stability. The • A741 is short-circuit-protected and allows for nulling of offset voltage.

PIN CONFIGURATION

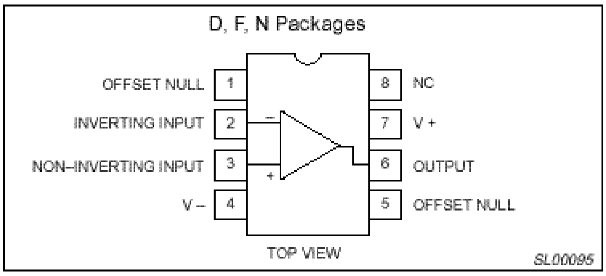

Figure 1. Pin Configuration

FEATURES

- Internal frequency compensation
- Short circuit protection
- Excellent temperature stability
- High input voltage range

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-55•C to +125•C	• A741N	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70•C	• A741CN	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	-40•C to +85•C	SA741CN	SOT97-1
8-Pin Ceramic Dual In-Line Package (CERDIP)	-55•C to +125•C	• A741F	0580A
8-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70•C	• A741CF	0580A
8-Pin Small Outline (SO) Package	0 to +70•C	• A741CD	SOT96-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage		
	• A741C	• 18	V
	• A741	• 22	V
P_D	Internal power dissipation		
	D package	780	mW
	N package	1170	mW
	F package	800	mW
V_{IN}	Differential input voltage	• 30	V
V_{IN}	Input voltage[1]	• 15	V
I_{SC}	Output short-circuit duration	Continuous	
T_A	Operating temperature range		
	• A741C	0 to +70	•C
	SA741C	-40 to +85	•C
	• A741	-55 to +125	•C
T_{STG}	Storage temperature range	-65 to +150	•C
T_{SOLD}	Lead soldering temperature (10sec max)	300	•C

NOTES:
1. For supply voltages less than • 15V, the absolute maximum input voltage is equal to the supply voltage.

OA741

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General purpose operational amplifier • A741/• A741C/SA741C

DC ELECTRICAL CHARACTERISTICS

T_A = 25•C, V_S = • 15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	• A741			• A741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	R_S=10k•		1.0	5.0		2.0	6.0	mV
		R_S=10k• , over temp.		1.0	6.0			7.5	mV
• V_{OS}/• T				10			10		• V/•C
I_{OS}	Offset current			20	200		20	200	nA
		Over temp.						300	nA
		T_A=+125•C		7.0	200				nA
		T_A=-55•C		20	500				nA
• I_{OS}/• T				200			200		pA/•C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temp.						800	nA
		T_A=+125•C		30	500				nA
		T_A=-55•C		300	1500				nA
• I_B/• T				1			1		nA/•C
V_{OUT}	Output voltage swing	R_L=10k•	• 12	• 14		• 12	• 14		V
		R_L=2k• , over temp.	• 10	• 13		• 10	• 13		V
A_{VOL}	Large-signal voltage gain	R_L=2k• , V_O=• 10V	50	200		20	200		V/mV
		R_L=2k• , V_O=• 10V, over temp.	25			15			V/mV
	Offset voltage adjustment range			• 30			• 30		mV
PSRR	Supply voltage rejection ratio	R_S• 10k•					10	150	• V/V
		R_S• 10k• , over temp.		10	150				• V/V
CMRR	Common-mode rejection ratio					70	90		dB
		Over temp.	70	90					dB
I_{CC}	Supply current			1.4	2.8		1.4	2.8	mA
		T_A=+125•C		1.5	2.5				mA
		T_A=-55•C		2.0	3.3				mA
V_{IN}	Input voltage range	(• A741, over temp.)	• 12	• 13		• 12	• 13		V
R_{IN}	Input resistance		0.3	2.0		0.3	2.0		M•
P_D	Power consumption			50	85		50	85	mW
		T_A=+125•C		45	75				mW
		T_A=-55•C		45	100				mW
R_{OUT}	Output resistance			75			75		•
I_{SC}	Output short-circuit current		10	25	60	10	25	60	mA

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General purpose operational amplifier • A741/• A741C/SA741C

DC ELECTRICAL CHARACTERISTICS

T_A = 25•C, V_S = • 15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA741C			UNIT
			Min	Typ	Max	
V_{OS}		R_S=10k•		2.0	6.0	mV
	Offset voltage	R_S=10k• , over temp.			7.5	mV
• V_{OS}/• T				10		• V/•C
I_{OS}				20	200	nA
	Offset current	Over temp.			500	nA
• I_{OS}/• T				200		pA/•C
I_{BIAS}				80	500	nA
	Input bias current	Over temp.			1500	nA
• I_B/• T				1		nA/•C
		R_L=10k•	• 12	• 14		V
V_{OUT}	Output voltage swing					
		R_L=2k• , over temp.	• 10	• 13		V
		R_L=2k• , V_O=• 10V	20	200		V/mV
A_{VOL}	Large-signal voltage gain					
		R_L=2k• , V_O=• 10V, over temp.	15			V/mV
	Offset voltage adjustment range			• 30		mV
PSRR	Supply voltage rejection ratio	R_S• 10k•		10	150	• V/V
CMRR	Common mode rejection ration		70	90		dB
V_{IN}	Input voltage range	Over temp.	• 12	• 13		V
R_{IN}	Input resistance		0.3	2.0		M•
P_d	Power consumption			50	85	mW
R_{OUT}	Output resistance			75		•
I_{SC}	Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS

T_A=25•C, V_S = • 15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	• A741, • A741C			UNIT
			Min	Typ	Max	
R_{IN}	Parallel input resistance	Open-loop, f=20Hz	0.3			M•
C_{IN}	Parallel input capacitance	Open-loop, f=20Hz		1.4		pF
	Unity gain crossover frequency	Open-loop		1.0		MHz
	Transient response unity gain	V_{IN}=20mV, R_L=2k• , C_L• 100pF				
t_R	Rise time			0.3		• s
	Overshoot			5.0		%
SR	Slew rate	C• 100pF, R_L• 2k• , V_{IN}=• 10V		0.5		V/• s

OA741

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General purpose operational amplifier • A741/• A741C/SA741C

EQUIVALENT SCHEMATIC

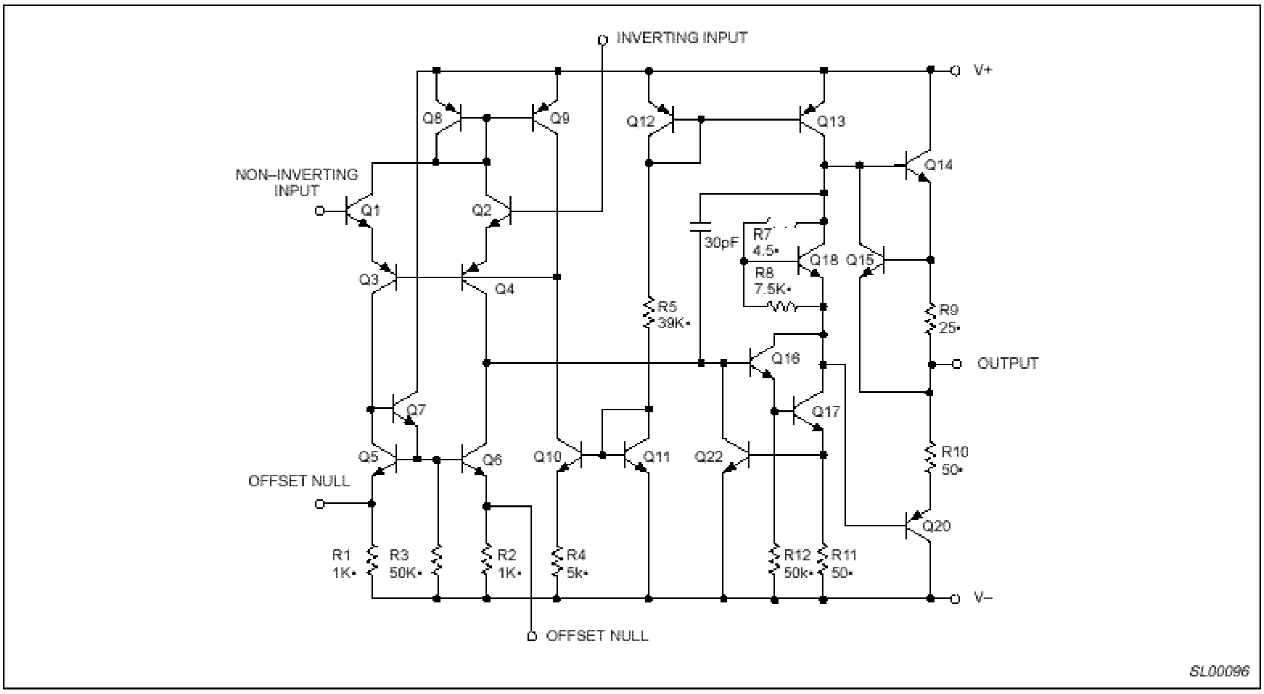

Figure 2. Equivalent Schematic

OA741

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General purpose operational amplifier • A741/• A741C/SA741C

TYPICAL PERFORMANCE CHARACTERISTICS

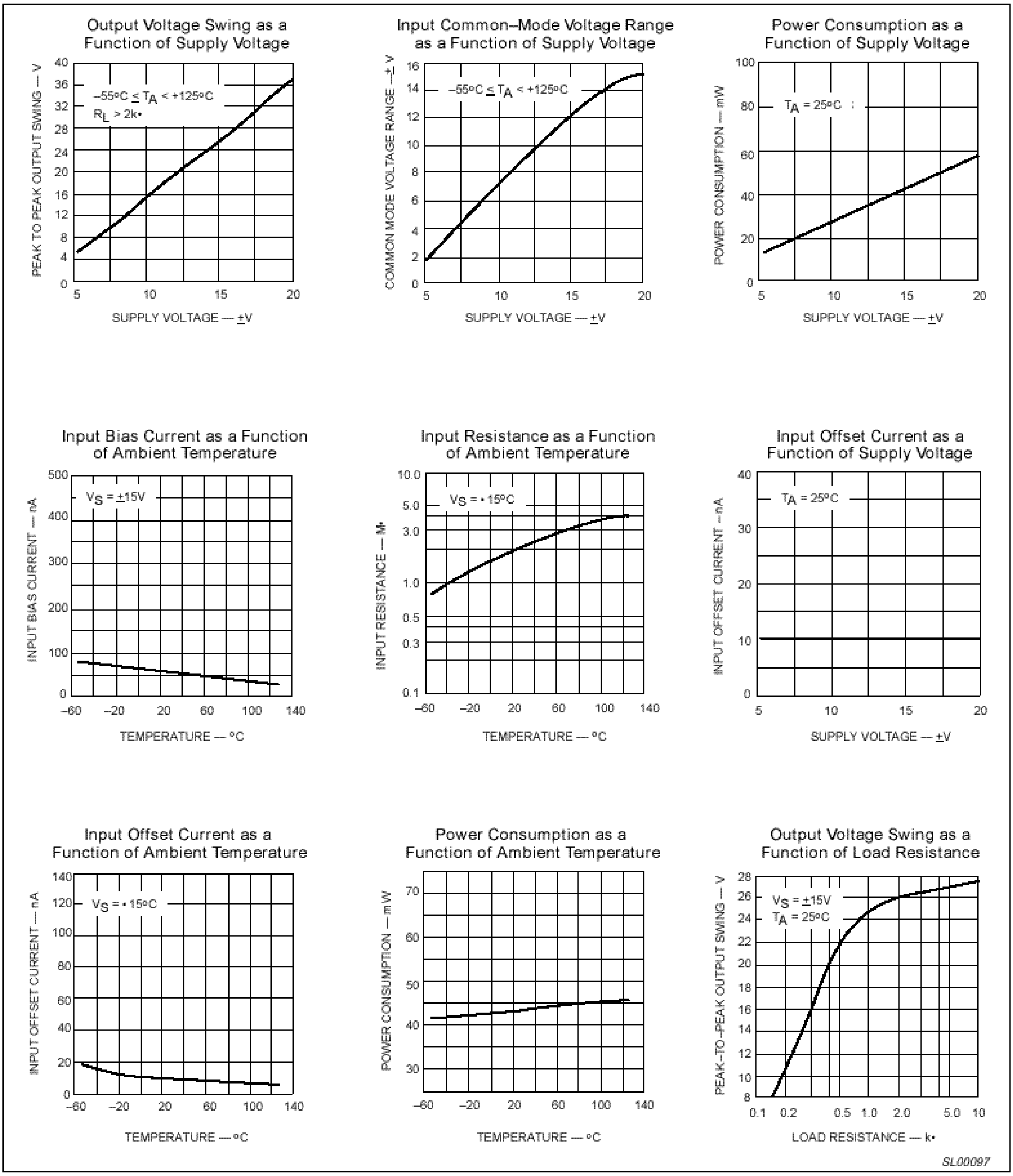

Figure 3. Typical Performance Characteristics

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General purpose operational amplifier • A741/• A741C/SA741C

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

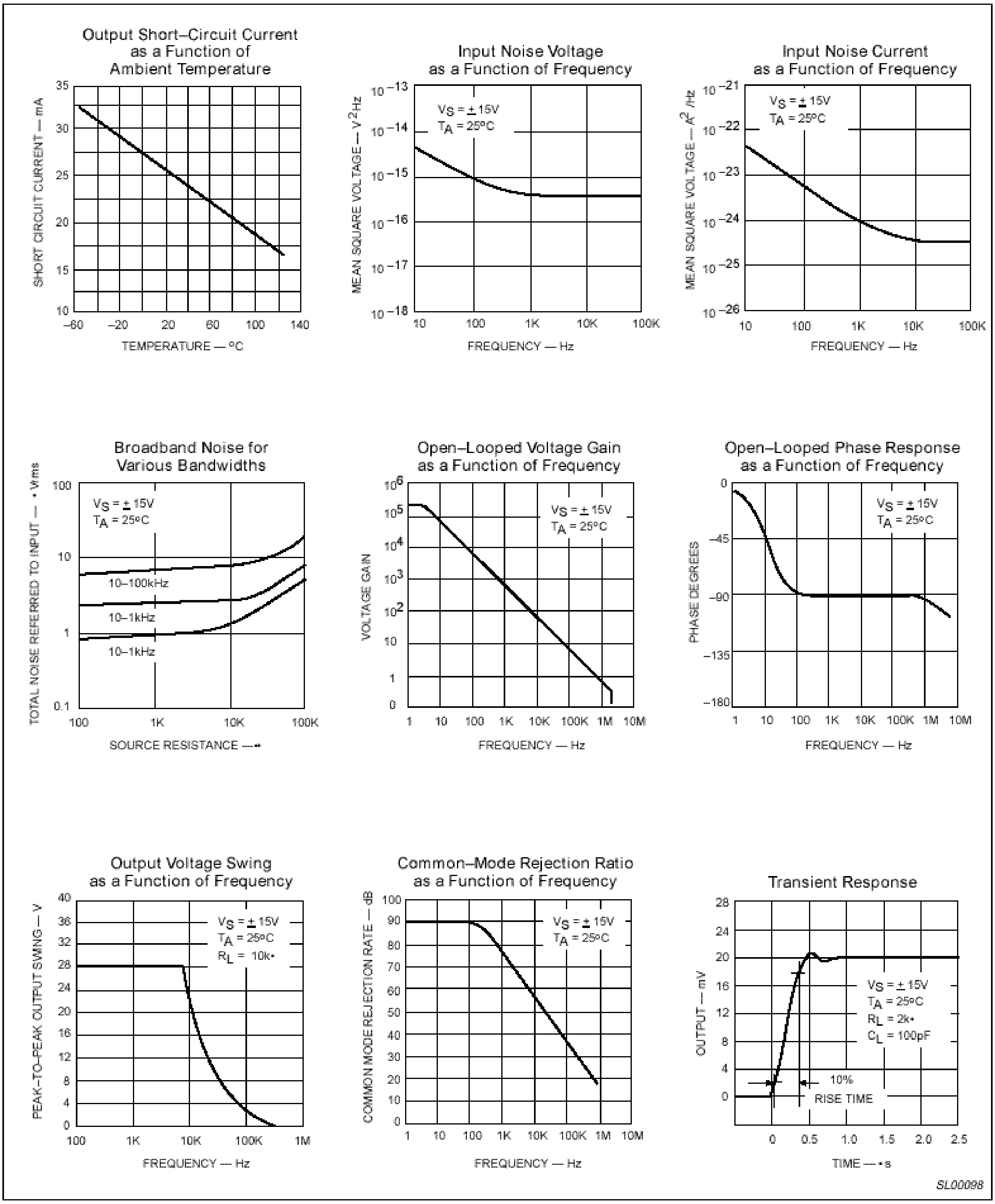

Figure 4. Typical Performance Characteristics (cont.)

OA741

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National Semiconductor

August 1999

LM117/LM317A/LM317
3-Terminal Adjustable Regulator

LM117/LM317A/LM317 3-Terminal Adjustable Regulator

General Description

The LM117 series of adjustable 3-terminal positive voltage regulators is capable of supplying in excess of 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., avoid short-circuiting the output.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

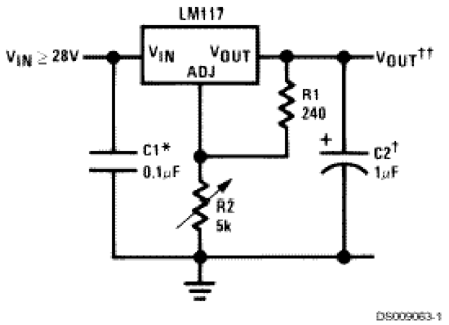
For applications requiring greater output current, see LM150 series (3A) and LM138 series (5A) data sheets. For the negative complement, see LM137 series data sheet.

Features

- Guaranteed 1% output voltage tolerance (LM317A)
- Guaranteed max. 0.01%/V line regulation (LM317A)
- Guaranteed max. 0.3% load regulation (LM117)
- Guaranteed 1.5A output current
- Adjustable output down to 1.2V
- Current limit constant with temperature
- P^+ Product Enhancement tested
- 80 dB ripple rejection
- Output is short-circuit protected

Typical Applications

1.2V–25V Adjustable Regulator



Full output current not available at high input-output voltages

*Needed if device is more than 6 inches from filter capacitors.

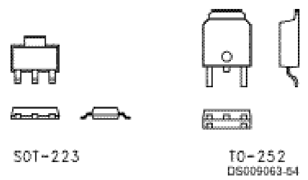
†Optional — improves transient response. Output capacitors in the range of 1 µF to 1000 µF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R_2)$$

LM117 Series Packages

Part Number Suffix	Package	Design Load Current
K	TO-3	1.5A
H	**TO-39**	**0.5A**
T	TO-220	1.5A
E	**LCC**	**0.5A**
S	TO-263	1.5A
EMP	SOT-223	1A
MDT	**TO-252**	**0.5A**

SOT-223 vs D-Pak (TO-252) Packages



Scale 1:1

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation	Internally Limited
Input-Output Voltage Differential	+40V, −0.3V
Storage Temperature	−65°C to +150°C
Lead Temperature	
Metal Package (Soldering, 10 seconds)	300°C
Plastic Package (Soldering, 4 seconds)	260°C
ESD Tolerance (Note 5)	3 kV

Operating Temperature Range

LM117	$-55°C \le T_J \le +150°C$
LM317A	$-40°C \le T_J \le +125°C$
LM317	$0°C \le T_J \le +125°C$

Preconditioning

Thermal Limit Burn-In	All Devices 100%

Electrical Characteristics (Note 3)

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V, and I_{OUT} = 10 mA.

Parameter	Conditions	LM117 (Note 2)			Units
		Min	Typ	Max	
Reference Voltage					V
	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $10\ mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	**1.20**	**1.25**	**1.30**	V
Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$ (Note 4)		0.01	0.02	%/V
			0.02	**0.05**	%/V
Load Regulation	$10\ mA \le I_{OUT} \le I_{MAX}$ (Note 4)		0.1	0.3	%
			0.3	**1**	%
Thermal Regulation	20 ms Pulse		0.03	0.07	%/W
Adjustment Pin Current			**50**	**100**	μA
Adjustment Pin Current Change	$10\ mA \le I_{OUT} \le I_{MAX}$, $3V \le (V_{IN} - V_{OUT}) \le 40V$		**0.2**	**5**	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		**1**		%
Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$		**3.5**	**5**	mA
Current Limit	$(V_{IN} - V_{OUT}) \le 15V$				
	K Package	**1.5**	**2.2**	**3.4**	A
	H Packages	**0.5**	**0.8**	**1.8**	A
	$(V_{IN} - V_{OUT}) = 40V$				
	K Package	0.3	0.4		A
	H Package	0.15	0.2		A
RMS Output Noise, % of V_{OUT}	$10\ Hz \le f \le 10\ kHz$		0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 μF		**65**		dB
	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 μF	**66**	**80**		dB
Long-Term Stability	T_J = 125°C, 1000 hrs		0.3	1	%
Thermal Resistance, Junction-to-Case	K Package		2.3	3	°C/W
	H Package		12	15	°C/W
	E Package				°C/W
Thermal Resistance, Junction-to-Ambient (No Heat Sink)	K Package		35		°C/W
	H Package		140		°C/W
	E Package				°C/W

LM117/317

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Application Hints

In operation, the LM117 develops a nominal 1.25V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

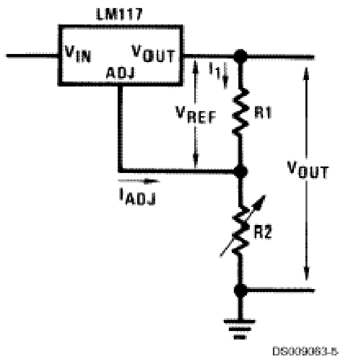

FIGURE 1.

Since the 100 µA current from the adjustment terminal represents an error term, the LM117 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

External Capacitors

An input bypass capacitor is recommended. A 0.1 µF disc or 1 µF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM117 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 µF bypass capacitor 80 dB ripple rejection is obtainable at any output level. Increases over 10 µF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use is solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 µF in aluminum electrolytic to equal 1 µF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 µF disc may seem to work better than a 0.1 µF disc as a bypass.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1 µF solid tantalum (or 25 µF aluminum electrolytic) on the output swamps this effect and insures stability. Any increase of the load capacitance larger than 10 µF will merely improve the loop stability and output impedance.

Load Regulation

The LM117 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output (case) of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω x I_L. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

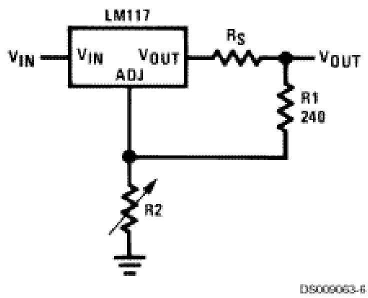

FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-39 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 µF capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_{IN}. In the LM117, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 µF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or

LM117/317

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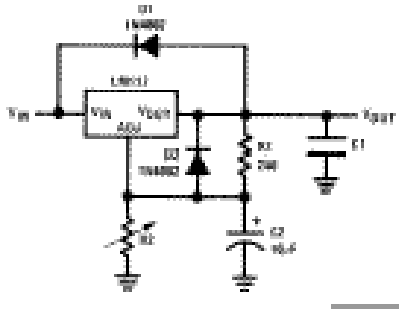
Application Hints (Continued)

less and 10 µF capacitance. *Figure 3* shows an LM117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



$$V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$$

D1 protects against C1
D2 protects against C2

FIGURE 3. Regulator with Protection Diodes

When a value for $\theta_{(H-A)}$ is found using the equation shown, *a heatsink must be selected that has a value that is less than or equal to this number.*

$\theta_{(H-A)}$ is specified numerically by the heatsink manufacturer in the catalog, or shown in a curve that plots temperature rise vs power dissipation for the heatsink.

HEATSINKING TO-263, SOT-223 AND TO-252 PACKAGE PARTS

The TO-263 ("S"), SOT-223 ("MP") and TO-252 ("DT") packages use a copper plane on the PCB and the PCB itself as a heatsink. To optimize the heat sinking ability of the plane and PCB, solder the tab of the package to the plane.

Figure 4 shows for the TO-263 the measured values of $\theta_{(J-A)}$ for different copper area sizes using a typical PCB with 1 ounce copper *and no solder mask over the copper area used for heatsinking.*

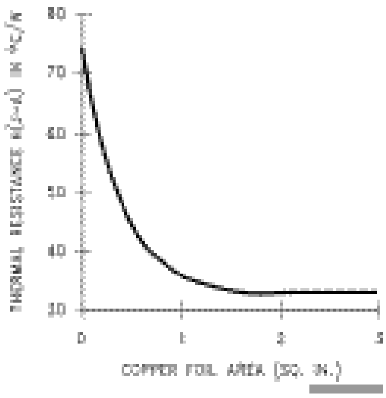


FIGURE 4. $\theta_{(J-A)}$ vs Copper (1 ounce) Area for the TO-263 Package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. It should also be observed that the minimum value of $\theta_{(J-A)}$ for the TO-263 package mounted to a PCB is 32˚C/W.

As a design aid, *Figure 5* shows the maximum allowable power dissipation compared to ambient temperature for the TO-263 device (assuming $\theta_{(J-A)}$ is 35˚C/W and the maximum junction temperature is 125˚C).

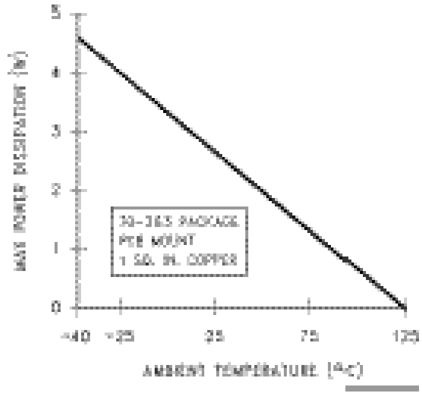


FIGURE 5. Maximum Power Dissipation vs T_{AMB} for the TO-263 Package

Figure 6 and *Figure 7* show the information for the SOT-223 package. *Figure 7* assumes a $\theta_{(J-A)}$ of 74˚C/W for 1 ounce copper and 51˚C/W for 2 ounce copper and a maximum junction temperature of 125˚C.

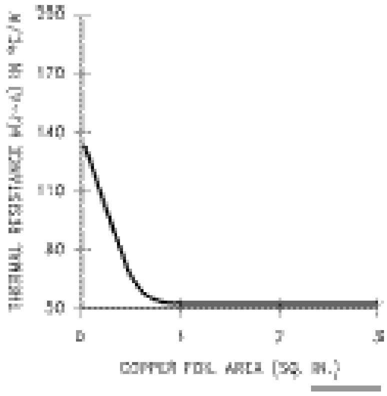


FIGURE 6. $\theta_{(J-A)}$ vs Copper (2 ounce) Area for the SOT-223 Package

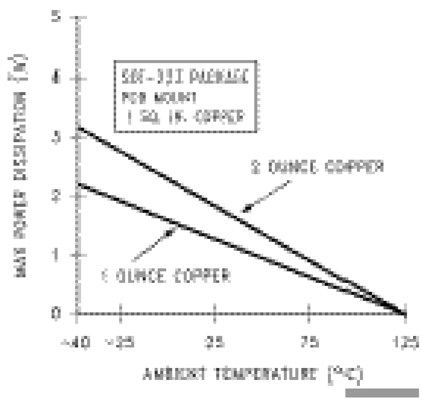


FIGURE 7. Maximum Power Dissipation vs T_{AMB} for the SOT-223 Package

LM117/317

I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

National Semiconductor

May 1999

LM137/LM337 3-Terminal Adjustable Negative Regulators

General Description

The LM137/LM337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

The LM137/LM337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137/LM337 are ideal complements to the LM117/LM317 adjustable positive regulators.

Features

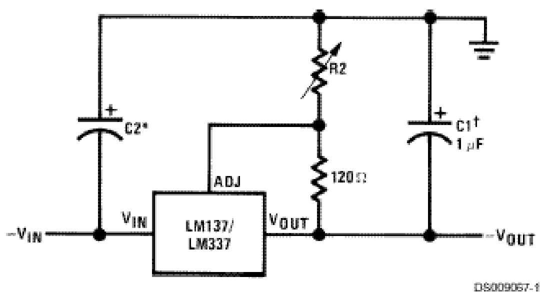
- Output voltage adjustable from −1.2V to −37V
- 1.5A output current guaranteed, −55˚C to +150˚C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/˚C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- P^+ Product Enhancement tested
- Standard 3-lead transistor package
- Output is short circuit protected

LM137 Series Packages and Power Capability

Device	Package	Rated Power Dissipation	Design Load Current
LM137/337	TO-3 (K)	20W	1.5A
	TO-39 (H)	2W	0.5A
LM337	TO-220 (T)	15W	1.5A
LM337	SOT-223 (MP)	2W	1A

Typical Applications

Adjustable Negative Voltage Regulator



Full output current not available at high input-output voltages

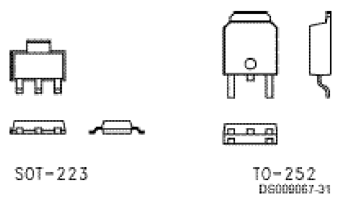
$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120}\right) + \left(-I_{ADJ} \times R2\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power-supply filter capacitor

Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients

Comparison between SOT-223 and D-Pak (TO-252) Packages



Scale 1:1

 I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

Absolute Maximum Ratings (Notes 1, 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation	Internally Limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	
LM137	−55°C to +150°C
LM337	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Plastic Package (Soldering, 4 sec.)	260°C
ESD Rating	2k Volts

Electrical Characteristics

(Note 1)

Parameter	Conditions	LM137			LM337			Units
		Min	Typ	Max	Min	Typ	Max	
Line Regulation	$T_j = 25°C$, $3V \le \lvert V_{IN} - V_{OUT}\rvert \le 40V$ (Note 2) $I_L = 10\ mA$		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_j = 25°C$, $10\ mA \le I_{OUT} \le I_{MAX}$		0.3	0.5		0.3	1.0	%
Thermal Regulation	$T_j = 25°C$, 10 ms Pulse		0.002	0.02		0.003	0.04	%/W
Adjustment Pin Current			65	100		65	100	μA
Adjustment Pin Current Charge	$10\ mA \le I_L \le I_{MAX}$ $3.0V \le \lvert V_{IN} - V_{OUT}\rvert \le 40V$, $T_A = 25°C$		2	5		2	5	μA
Reference Voltage	$T_j = 25°C$ (Note 3) $3V \le \lvert V_{IN} - V_{OUT}\rvert \le 40V$, (Note 3) $10\ mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	−1.225 −1.200	−1.250 −1.250	−1.275 −1.300	−1.213 −1.200	−1.250 −1.250	−1.287 −1.300	V V
Line Regulation	$3V \le \lvert V_{IN} - V_{OUT}\rvert \le 40V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\ mA \le I_{OUT} \le I_{MAX}$, (Note 2)		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.6			0.6		%
Minimum Load Current	$\lvert V_{IN} - V_{OUT}\rvert \le 40V$ $\lvert V_{IN} - V_{OUT}\rvert \le 10V$		2.5 1.2	5 3		2.5 1.5	10 6	mA mA
Current Limit	$\lvert V_{IN} - V_{OUT}\rvert \le 15V$ K, MP and T Package H Package $\lvert V_{IN} - V_{OUT}\rvert = 40V$, $T_j = 25°C$ K, MP and T Package H Package	 1.5 0.5 0.24 0.15	 2.2 0.8 0.4 0.17	 3.5 1.8	 1.5 0.5 0.15 0.10	 2.2 0.8 0.4 0.17	 3.7 1.9	 A A A A
RMS Output Noise, % of V_{OUT}	$T_j = 25°C$, $10\ Hz \le f \le 10\ kHz$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, f = 120 Hz $C_{ADJ} = 10\ \mu F$	 66	60 77		 66	60 77		dB dB
Long-Term Stability	$T_j = 125°C$, 1000 Hours		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package K Package T Package		12 2.3	15 3		12 2.3 4	15 3	°C/W °C/W °C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	H Package K Package T Package MP Package		140 35			140 35 50 170		°C/W °C/W °C/W °C/W

Note 1: Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM137, $0°C \le T_j \le +125°C$ for the LM337; $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 package and $I_{OUT} = 0.5A$ for the TO-3, SOT-223 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and SOT-223 (see Application Hints), and 20W for the TO-3, and TO-220. I_{MAX} is 1.5A for the TO-3, SOT-223 and TO-220 packages, and 0.2A for the TO-39 package.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point ⅛" below the base of the TO-3 and TO-39 packages.

Note 3: Selected devices with tightened tolerance reference voltage available.

Note 4: Refer to RETS137H drawing for LM137H or RETS137K drawing for LM137K military specifications.

LM137/337

I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

Application Hints (Continued)

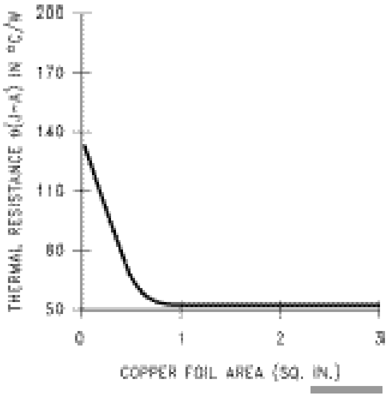


FIGURE 3. $\theta_{(J-A)}$ **vs Copper (2 ounce) Area for the SOT-223 Package**

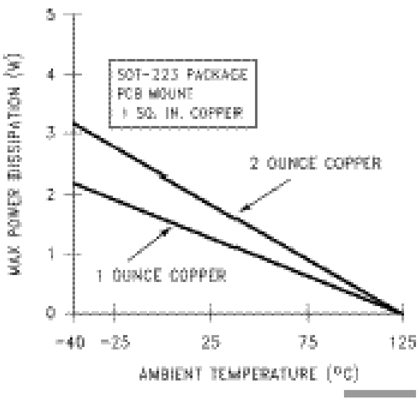
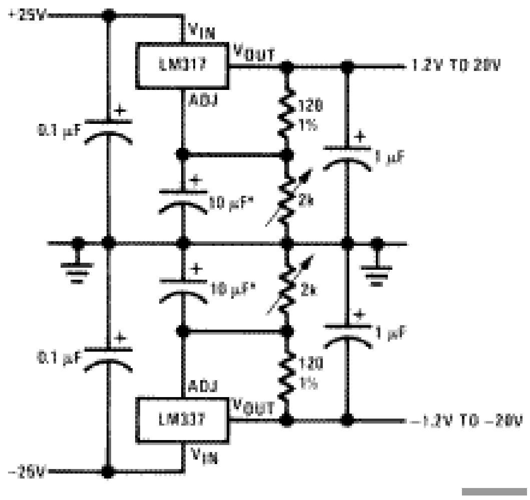


FIGURE 4. Maximum Power Dissipation vs T_{AMB} **for the SOT-223 Package**

Please see AN1028 for power enhancement techniques to be used with the SOT-223 package.

Typical Applications

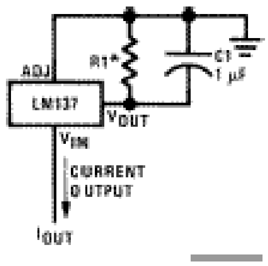
Adjustable Lab Voltage Regulator



Full output current not available at high input-output voltages

*The 10 µF capacitors are optional to improve ripple rejection

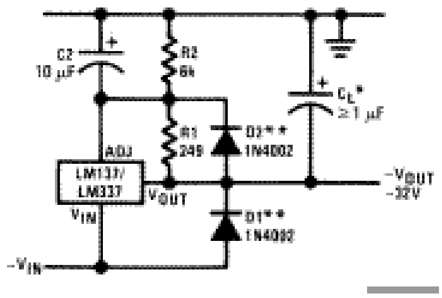
Current Regulator



$I_{OUT} = \frac{1.250V}{R1}$

*0.8Ω ≤ R1 ≤ 120Ω

Negative Regulator with Protection Diodes



*When C_L is larger than 20 µF, D1 protects the LM137 in case the input supply is shorted

**When C2 is larger than 10 µF and $-V_{OUT}$ is larger than −25V, D2 protects the LM137 in case the output is shorted

LM137/337

I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

MKP3V120, MKP3V240

Preferred Device

Sidac High Voltage

Bidirectional Triggers

Bidirectional devices designed for direct interface with the ac power line. Upon reaching the breakover voltage in each direction, the device switches from a blocking state to a low voltage on–state. Conduction will continue like a Triac until the main terminal current drops below the holding current. The plastic axial lead package provides high pulse current capability at low cost. Glass passivation insures reliable operation. Applications are:

- High Pressure Sodium Vapor Lighting
- Strobes and Flashers
- Ignitors
- High Voltage Regulators
- Pulse Generators
- Used to Trigger Gates of SCR's and Triacs
- UL Indicates UL Registered — File #E116110
- Device Marking: Logo, Device Type, e.g., MKP3V120, Date Code

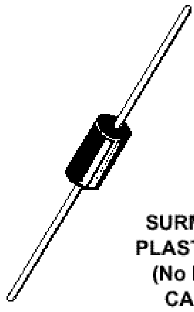
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage (Sine Wave, 50 to 60 Hz, T_J = −40 to 125°C) MKP3V120 / MKP3V240	V_{DRM}, V_{RRM}	±90 / ±180	Volts
On-State RMS Current (T_L = 80°C, Lead Length = 3/8″, All Conduction Angles)	$I_{T(RMS)}$	±1.0	Amp
Peak Non–Repetitive Surge Current (60 Hz One Cycle Sine Wave, Peak Value, T_J = 125°C)	I_{TSM}	±20	Amps
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

ON Semiconductor

http://onsemi.com

SIDACS (UL)
1 AMPERE RMS
120 and 240 VOLTS



SURMETIC 50
PLASTIC AXIAL
(No Polarity)
CASE 267
STYLE 2

ORDERING INFORMATION

Device	Package	Shipping
MKP3V120	SURMETIC 50	Bulk 500/Bag
MKP3V120RL	SURMETIC 50	Tape and Reel 1.5K/Reel
MKP3V240	SURMETIC 50	Bulk 500/Bag
MKP3V240RL	SURMETIC 50	Tape and Reel 1.5K/Reel

Preferred devices are recommended choices for future use and best overall value.

MKP3V129/240

I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

MKP3V120, MKP3V240

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Lead (Lead Length = 3/8″)	$R_{\theta JL}$	15	°C/W
Lead Solder Temperature (Lead Length ≥ 1/16″ from Case, 10 s Max)	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Repetitive Peak Off–State Current (50 to 60 Hz Sine Wave) V_{DRM} = 90 V MKP3V120 V_{DRM} = 180 V MKP3V240	I_{DRM}	—	—	10	µA
ON CHARACTERISTICS					
Breakover Voltage, I_{BO} = 200 µA MKP3V120 MKP3V240	V_{BO}	 110 220	 — —	 130 250	Volts
Breakover Current	I_{BO}	—	—	200	µA
Peak On–State Voltage (I_{TM} = 1 A Peak, Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%)	V_{TM}	—	1.1	1.5	Volts
Dynamic Holding Current (Sine Wave, 60 Hz, R_L = 100 Ω)	I_H	—	—	100	mA
Switching Resistance (Sine Wave, 50 to 60 Hz)	R_S	0.1	—	—	kΩ
DYNAMIC CHARACTERISTICS					
Critical Rate–of–Rise of On–State Current, Critical Damped Waveform Circuit (I_{PK} = 130 Amps, Pulse Width = 10 µsec)	di/dt	—	120	—	A/µs

MKP3V129/240

I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document
by MBS4991/D

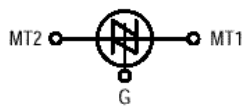
MBS4991
MBS4992
MBS4993

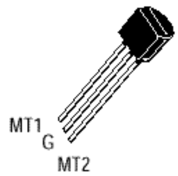
Silicon Bidirectional Switches
Diode Thyristors

. . . designed for full-wave triggering in Triac phase control circuits, half-wave SCR triggering application and as voltage level detectors. Supplied in an inexpensive plastic TO-226AA package for high-volume requirements, this low-cost plastic package is readily adaptable for use in automatic insertion equipment.

- Low Switching Voltage — 8 Volts Typical
- Uniform Characteristics in Each Direction
- Low On-State Voltage — 1.7 Volts Maximum
- Low Off-State Current — 0.1 µA Maximum
- Low Temperature Coefficient — 0.02 %/°C Typical

SBS
(PLASTIC)





CASE 29-04
(TO-226AA)
STYLE 12

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Dissipation	P_D	500	mW
DC Forward Current	I_F	200	mA
DC Gate Current (Off-State Only)	I_G(off)	5	mA
Repetitive Peak Forward Current (1% Duty Cycle, 10 µs Pulse Width, T_A = 100°C)	I_{FM}(rep)	2	Amps
Non-repetitive Forward Current (10 µs Pulse Width, T_A = 25°C)	I_{FM}(nonrep)	6	Amps
Operating Junction Temperature Range	T_J	–55 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

MBS4991/2/3

I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

MBS4991 MBS4992 MBS4993

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Switching Voltage	MBS4991 MBS4992, MBS4993	V_S	6 7.5	8 8	10 9	Vdc
Switching Current	MBS4991 MBS4992 MBS4993	I_S	— —	175 90 175	500 120 250	μAdc
Switching Voltage Differential (See Figure 10)	MBS4991 MBS4992, MBS4993	$\|V_{S1}–V_{S2}\|$	— —	0.3 0.1	0.5 0.2	Vdc
Gate Trigger Current (V_F = 5 Vdc, R_L = 1 k ohm)	MBS4992 MBS4993	I_{GF}	— —	— —	100 500	μAdc
Holding Current	MBS4991 MBS4992 MBS4993	I_H	— — —	0.7 0.2 0.3	1.5 0.5 0.75	mAdc
Off-State Blocking Current (V_F = 5 Vdc, T_A = 25°C) (V_F = 5 Vdc, T_A = 85°C) (V_F = 5 Vdc, T_A = 25°C) (V_F = 5 Vdc, T_A = 100°C)	 MBS4991 MBS4991 MBS4992, MBS4993 MBS4992, MBS4993	I_B	 — — — —	 0.08 2 0.08 6	 1 10 0.1 10	μAdc
Forward On-State Voltage (I_F = 175 mAdc) (I_F = 200 mAdc)	 MBS4991 MBS4992, MBS4993	V_F	 — —	 1.4 1.5	 1.7 1.7	Vdc
Peak Output Voltage (C_C = 0.1 μF, R_L = 20 ohms, (Figure 7)		V_o	3.5	4.8	—	Vdc
Turn-On Time (Figure 8)		t_{on}	—	1	—	μs
Turn-Off Time (Figure 9)		t_{off}	—	30	—	μs
Temperature Coefficient of Switching Voltage (–50 to +125°C)		T_C	—	+0.02	—	%/°C
Switching Current Differential (See Figure 10)		$I_{S1}–I_{S2}$	—	—	100	μA

MBS4991/2/3

I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

2N5060 Series

Preferred Device

Sensitive Gate Silicon Controlled Rectifiers

Reverse Blocking Thyristors

Annular PNPN devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-226AA (TO-92) package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current — 200 µA Maximum
- Low Reverse and Forward Blocking Current — 50 µA Maximum, T_C = 110°C
- Low Holding Current — 5 mA Maximum
- Passivated Surface for Reliability and Uniformity
- Device Marking: Device Type, e.g., 2N5060, Date Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage(1) (T_J = −40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open) 2N5060 / 2N5061 / 2N5062 / 2N5064	V_{DRM}, V_{RRM}	30 / 60 / 100 / 200	Volts
On-State Current RMS (180° Conduction Angles; T_C = 80°C)	$I_{T(RMS)}$	0.8	Amp
*Average On-State Current (180° Conduction Angles) (T_C = 67°C) / (T_C = 102°C)	$I_{T(AV)}$	0.51 / 0.255	Amp
*Peak Non-repetitive Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	0.4	A^2s
*Forward Peak Gate Power (Pulse Width ≤ 1.0 µsec; T_A = 25°C)	P_{GM}	0.1	Watt
*Forward Average Gate Power (T_A = 25°C, t = 8.3 ms)	$P_{G(AV)}$	0.01	Watt
*Forward Peak Gate Current (Pulse Width ≤ 1.0 µsec; T_A = 25°C)	I_{GM}	1.0	Amp
*Reverse Peak Gate Voltage (Pulse Width ≤ 1.0 µsec; T_A = 25°C)	V_{RGM}	5.0	Volts
*Operating Junction Temperature Range	T_J	–40 to +110	°C
*Storage Temperature Range	T_{stg}	–40 to +150	°C

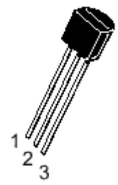
*Indicates JEDEC Registered Data.

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

ON Semiconductor

http://onsemi.com

SCRs
0.8 AMPERES RMS
30 thru 200 VOLTS



TO–92 (TO–226AA)
CASE 029
STYLE 10

PIN ASSIGNMENT	
1	Cathode
2	Gate
3	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

2N5060

2N5060 Series

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case(1)	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
*Lead Solder Temperature (Lead Length ≥ 1/16″ from case, 10 s Max)	—	+230*	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
*Peak Repetitive Forward or Reverse Blocking Current(2) (V_{AK} = Rated V_{DRM} or V_{RRM})	T_C = 25°C	I_{DRM}, I_{RRM}	—	—	10	μA
	T_C = 110°C		—	—	50	μA
ON CHARACTERISTICS						
*Peak Forward On–State Voltage(3) (I_{TM} = 1.2 A peak @ T_A = 25°C)		V_{TM}	—	—	1.7	Volts
Gate Trigger Current (Continuous dc)(4) *(V_{AK} = 7 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	—	—	200	μA
	T_C = –40°C		—	—	350	
Gate Trigger Voltage (Continuous dc)(4) *(V_{AK} = 7 Vdc, R_L = 100 Ohms)	T_C = 25°C	V_{GT}	—	—	0.8	Volts
	T_C = –40°C		—	—	1.2	
*Gate Non–Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 110°C	V_{GD}	0.1	—	—	Volts
Holding Current(4) *(V_{AK} = 7 Vdc, initiating current = 20 mA)	T_C = 25°C	I_H	—	—	5.0	mA
	T_C = –40°C		—	—	10	
Turn-On Time						μs
Delay Time		t_d	—	3.0	—	
Rise Time (I_{GT} = 1 mA, V_D = Rated V_{DRM}, Forward Current = 1 A, di/dt = 6 A/μs		t_r	—	0.2	—	
Turn-Off Time (Forward Current = 1 A pulse, Pulse Width = 50 μs, 0.1% Duty Cycle, di/dt = 6 A/μs, dv/dt = 20 V/μs, I_{GT} = 1 mA)	2N5060, 2N5061	t_q	—	10	—	μs
	2N5062, 2N5064		—	30	—	
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off–State Voltage (Rated V_{DRM}, Exponential)		dv/dt	—	30	—	V/μs

*Indicates JEDEC Registered Data.

(1) This measurement is made with the case mounted "flat side down" on a heat sink and held in position by means of a metal clamp over the curved surface.
(2) R_{GK} = 1000 Ω is included in measurement.
(3) Forward current applied for 1 ms maximum duration, duty cycle ≤ 1%.
(4) R_{GK} current is not included in measurement.

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2N5060

I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

2N6027, 2N6028

Preferred Device

Programmable Unijunction Transistor

Programmable Unijunction Transistor Triggers

Designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor–trigger, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO–92 plastic package for high–volume requirements, this package is readily adaptable for use in automatic insertion equipment.

- Programmable — R_{BB}, η, I_V and I_P
- Low On–State Voltage — 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current — 10 nA Maximum
- High Peak Output Voltage — 11 Volts Typical
- Low Offset Voltage — 0.35 Volt Typical (R_G = 10 k ohms)
- Device Marking: Logo, Device Type, e.g., 2N6027, Date Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
*Power Dissipation Derate Above 25°C	P_F $1/\theta_{JA}$	300 4.0	mW mW/°C
*DC Forward Anode Current Derate Above 25°C	I_T	150 2.67	mA mA/°C
*DC Gate Current	I_G	±50	mA
Repetitive Peak Forward Current 100 µs Pulse Width, 1% Duty Cycle *20 µs Pulse Width, 1% Duty Cycle	I_{TRM}	 1.0 2.0	Amps
Non–Repetitive Peak Forward Current 10 µs Pulse Width	I_{TSM}	5.0	Amps
*Gate to Cathode Forward Voltage	V_{GKF}	40	Volts
*Gate to Cathode Reverse Voltage	V_{GKR}	–5.0	Volts
*Gate to Anode Reverse Voltage	V_{GAR}	40	Volts
*Anode to Cathode Voltage(1)	V_{AK}	±40	Volts
Operating Junction Temperature Range	T_J	–50 to +100	°C
*Storage Temperature Range	T_{stg}	–55 to +150	°C

*Indicates JEDEC Registered Data

(1) Anode positive, R_{GA} = 1000 ohms
Anode negative, R_{GA} = open

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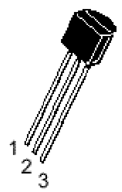
PUTs
40 VOLTS
300 mW



TO–92 (TO–226AA)
CASE 029
STYLE 16

PIN ASSIGNMENT	
1	Anode
2	Gate
3	Cathode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

2N6027/28

 I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

THERMAL CHARACTERISTICS

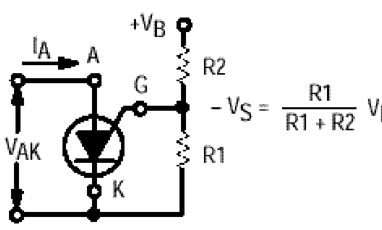
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Maximum Lead Temperature for Soldering Purposes (< 1/16″ from case, 10 secs max)	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

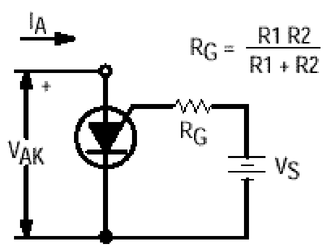
Characteristic	Fig. No.	Symbol	Min	Typ	Max	Unit
*Peak Current	2,9,11	I_P				μA
(V_S = 10 Vdc, R_G = 1 MΩ) 2N6027			—	1.25	2.0	
2N6028			—	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms) 2N6027			—	4.0	5.0	
2N6028			—	0.70	1.0	
*Offset Voltage	1	V_T				Volts
(V_S = 10 Vdc, R_G = 1 MΩ) 2N6027			0.2	0.70	1.6	
2N6028			0.2	0.50	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms) (Both Types)			0.2	0.35	0.6	
*Valley Current	1,4,5	I_V				μA
(V_S = 10 Vdc, R_G = 1 MΩ) 2N6027			—	18	50	
2N6028			—	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms) 2N6027			70	150	—	
2N6028			25	150	—	
(V_S = 10 Vdc, R_G = 200 ohms) 2N6027			1.5	—	—	mA
2N6028			1.0	—	—	
*Gate to Anode Leakage Current	—	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)			—	1.0	10	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)			—	3.0	—	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)	—	I_{GKS}	—	5.0	50	nAdc
*Forward Voltage (I_F = 50 mA Peak)(1)	1,6	V_F	—	0.8	1.5	Volts
*Peak Output Voltage (V_G = 20 Vdc, C_C = 0.2 μF)	3,7	V_o	6.0	11	—	Volt
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)	3	t_r	—	40	80	ns

*Indicates JEDEC Registered Data

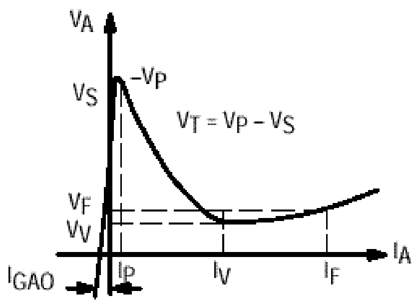
(1) Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.



1A – Programmable Unijunction with "Program" Resistors R1 and R2



1B – Equivalent Test Circuit for Figure 1A used for electrical characteristics testing (also see Figure 2)



IC – Electrical Characteristics

2N6027/28

2N2646

SILICON PN UNIJUNCTION TRANSISTOR

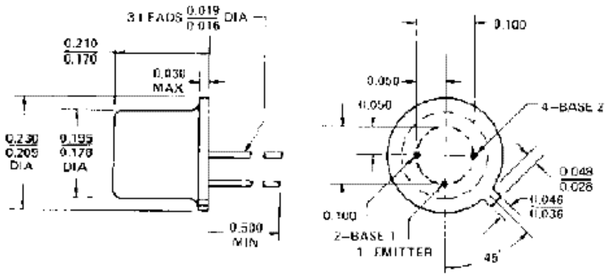
DESCRIPTION:

The **2N2646** is a Unijunction Transistor Used in General Purpose Pulse, Timing, Sense and Trigger Applications.

MAXIMUM RATINGS

I_C	2.0 A (PULSED)
V_{CE}	30 V
P_{DISS}	300 mW @ T_C = 25 ^{O}C
T_J	-65 ^{O}C to +125 ^{O}C
T_{STG}	-65 ^{O}C to +150 ^{O}C
θ_{JC}	33 ^{O}C/W

PACKAGE STYLE TO-18 (MOD)



CHARACTERISTICS T_C = 25 ^{O}C

SYMBOL	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
η	V_{B2B1} = 10 V	0.56		0.75	--
r_{BB}	V_{B2B1} = 3.0 V	4.7		9.1	KΩ
α_{rBB}	V_{B2B1} = 3.0 V T_A = -55 to 125^{O}C	0.1		0.9	%/°C
$V_{EB1(SAT)}$	V_{B2B1} = 10 V I_E = 50 mA		3.0		V
$I_{B2(MOD)}$	V_{B2B1} = 10 V I_E = 50 mA		20		mA
I_{B2EO}	V_{B2E} = 30 V I_{B1} = 0			12	µA
I_P	V_{B2B1} = 25 V			5.0	µA
I_V	V_{B2B1} = 20 V R_{B2} = 100 Ω	4.0			mA
V_{OB1}	V_{B2B1} = 20 V R_{B1} = 20 Ω	3.0	5.0		V

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MAC218A6FP, MAC218A10FP

Preferred Device

Triacs

Silicon Bidirectional Thyristors

Designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 800 Volts
- Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Isolated TO–220 Type Package for Ease of Mounting
- Gate Triggering Guaranteed in Four Modes
- UL Indicates UL Registered — File #E69369
- Device Marking: Logo, Device Type, e.g., MAC218A6FP, Date Code

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off–State Voltage(1) (T_J = –40 to +125°C, Sine Wave 50 to 60 Hz, Gate Open) MAC218A6FP MAC218A10FP	V_{DRM}, V_{RRM}	400 800	Volts
On-State RMS Current (T_C = +80°C)(2) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	8.0	Amps
Peak Non–Repetitive Surge Current (One Full Cycle, 60 Hz, T_C = +80°C) Preceded and followed by rated current	I_{TSM}	100	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	40	A^2s
Peak Gate Power (T_C = +80°C, Pulse Width = 10 μs)	P_{GM}	16	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Current (T_C = +80°C, Pulse Width = 10 μs)	I_{GM}	4.0	Amps
RMS Isolation Voltage (T_A = 25°C, Relative Humidity ≤ 20%) (UL)	$V_{(ISO)}$	1500	Volts
Operating Junction Temperature	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.
(2) The case temperature reference point for all T_C measurements is a point on the center lead of the package as close as possible to the plastic body.

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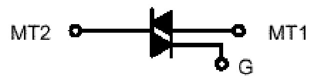
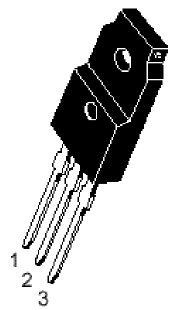
ISOLATED TRIAC (UL)
8 AMPERES RMS
400 thru 800 VOLTS





ISOLATED TO–220 Full Pack
CASE 221C
STYLE 3

PIN ASSIGNMENT	
1	Main Terminal 1
2	Main Terminal 2
3	Gate

ORDERING INFORMATION

Device	Package	Shipping
MAC218A6FP	ISOLATED TO220FP	500/Box
MAC218A10FP	ISOLATED TO220FP	500/Box

Preferred devices are recommended choices for future use and best overall value.

MAC218A

I.S.B.N.:84-607-1933-2 Depósito Legal:SA-138-2001

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Case to Sink	$R_{\theta CS}$	2.2 (typ)	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, V_{RRM}; Gate Open) T_J = 25°	I_{DRM}, I_{RRM}	—	—	10	µA
T_J = 125°C		—	—	2.0	mA
ON CHARACTERISTICS					
Peak On-State Voltage(1) (I_{TM} = ±11.3 A Peak)	V_{TM}	—	1.7	2.0	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ω)	I_{GT}				mA
MT2(+), G(+)		—	—	50	
MT2(+), G(–)		—	—	50	
MT2(–), G(–)		—	—	50	
MT2(–), G(+)		—	—	75	
Gate Trigger Voltage (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms)	V_{GT}				Volts
MT2(+), G(+)		—	0.9	2.0	
MT2(+), G(–)		—	0.9	2.0	
MT2(–), G(–)		—	1.1	2.0	
MT2(–), G(+)		—	1.4	2.5	
Gate Non–Trigger Voltage (Continuous dc) (Main Terminal Voltage = 12 V, R_L = 100 Ω, T_J = +125°C) All Four Quadrants	V_{GD}	0.2	—	—	Volts
Holding Current (V_D = 12 Vdc, Gate Open, Initiating Current = ±200 mA)	I_H	—	—	50	mA
DYNAMIC CHARACTERISTICS					
Critical Rate of Rise of Commutating Off–State Voltage (V_D = Rated V_{DRM}, I_{TM} = 11.3 A, Commutating di/dt = 4.1 A/ms, Gate Unenergized, T_C = 80°C)	$dv/dt_{(c)}$	—	5.0	—	V/µs
Critical Rate of Rise of Off–State Voltage (V_D = Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_J = 125°C)	dv/dt	—	100	—	V/µs

(1) Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

MAC218A

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